ST.ANNE'S

COLLEGE OF ENGINEERING AND TECHNOLOGY

(Approved by AICTE, New Delhi. Affiliated to Anna University, Chennai)

(An ISO 9001: 2015 Certified Institution)

ANGUCHETTYPALAYAM, PANRUTI - 607 110

2017 REGULATION

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING.

EC8261 CIRCUITS AND DEVICES LABORATORY

(I B.E II Semester Batch 2020-2024)

EC8261 CIRCUITS AND DEVICES LABORATORY

List of Experiments

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2. Characteristics of Zener diode
3. Characteristics of CE configuration.
4. Characteristics of CB configuration.
5. A.Characteristics of JFET .
   B. Characteristics of MOSFET
6. Characteristics of SCR
7. A. Characteristics of Clipper
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8. A.Verification of Thevenin Theorems.
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9. A. Verification of KVL
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10. Verification of Superposition Theorem.
11. A. Verification of Maximum Power Transfer
    B. Verification of reciprocity Theorems.
12. Frequency response of series & parallel resonance circuits.
13. Transient analysis of RL and RC circuits

CHARACTERISTICS OF PN DIODE

EX. NO: 1

AIM:

To determine the forward and reverse characteristics of a PN diode.

APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1	RPS	(0-30)V	1
2	Resistor	220Ω	1
3	DC Voltmeter	(0-1)V	1
4	DC Ammeter	(0-100)mA	1
5	Diode	IN4007	1
6	Bread board	-	1
7	Connecting wires	-	Few

THEORY:

A semiconductor diode's current–voltage characteristic, or I–V curve, is related to the transport of carriers through the so-called depletion layer or depletion region that exists at the p-n junction between differing semiconductors.

If an external voltage is placed across the diode, an increasing electric field develops through the depletion zone which acts to slow and then finally stop recombination. At this point, there is a "built-in" potential across the depletion zone.

If an external voltage across the diode with the same polarity as the built-in potential, the depletion zone continues to act as an insulator, preventing any significant electric current flow. This is the reverse bias phenomenon.

However, if the polarity of the external voltage opposes the built-in potential, recombination can once again proceed, resulting in substantial electric current through the p-n junction. For silicon diodes, the built-in potential is
approximately 0.6 V. Thus, if an external current is passed through the diode, about 0.6 V will be developed across the diode such that the P-doped region is positive with respect to

the N-doped region and the diode is said to be "turned on" as it has a forward bias.

At very large reverse bias, beyond the peak inverse voltage or PIV, a process called reverse breakdown occurs which causes a large increase in current that usually damages the device permanently. Also, following the end of forward conduction in any diode, there is reverse current for a short time. The device does not attain its full blocking capability until the reverse current ceases.

The second region, at reverse biases more positive than the PIV, has only a very small reverse saturation current. The third region is forward but small bias, where only a small forward current is conducted.

As the potential difference is increased above an arbitrarily defined "cut-in voltage" or "on-voltage" or "diode forward voltage drop (Vd)", the diode current becomes appreciable, and the diode presents a very low resistance.

The current–voltage curve is exponential. In a normal silicon diode at rated currents, the arbitrary "cut-in" voltage is defined as 0.6 to 0.7 volts. The value is different for other diode types — Schottky diodes can be as low as 0.2 V and red light-emitting diodes (LEDs) can be 1.4 V or more and blue LEDs can be up to 4.0 V.

At higher currents the forward voltage drop of the diode increases. A drop of 1 V to 1.5 V is typical at full rated current for power diodes.

V-I Characteristic equation or diode current equation is,

$$I = I_0 \left[e^{V/\eta V_T} - 1 \right] \; Amps$$

Where, $I_0 = reverse\ saturation\ current\ in\ amperes$

V = Applied voltage

= Efficiency (1 for germanium diode;

= kT volts

Where, k = Boltzmann's constant = 8.62 X 10^{-5} eV/^{0}K T = Temperature in ^{0}K

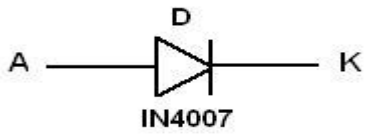
At room temperature of 27^{0}C,

T = 27 + 273 = 300 ^{0}K

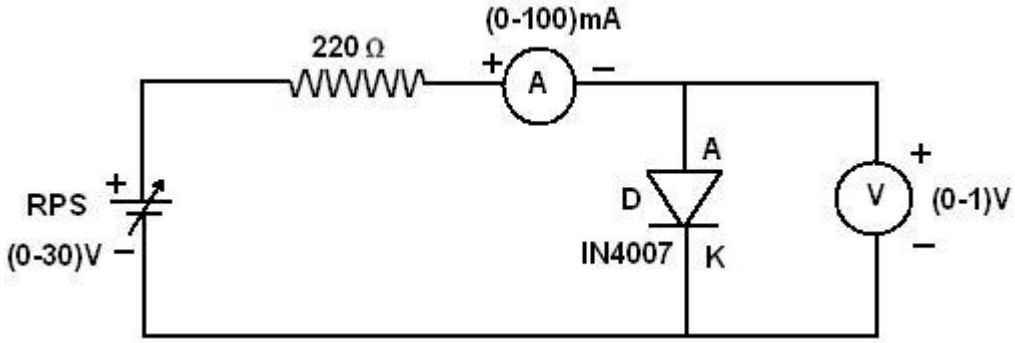
$\therefore V_T = 8.62 \text{ X } 10^{-5} \text{ X } 300$

= 25.86 mV

SEMICONDUCTOR DIODE:



FORWARD BIAS CHARACTERISTICS:



Circuit Diagram for Forward Bias

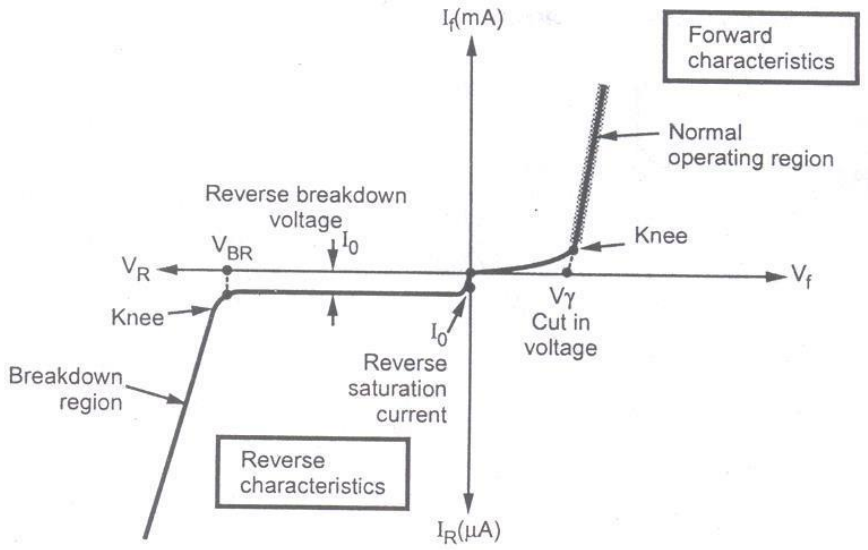
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. Power supply is switched ON.
3. By varying the RPS, the forward current is noted for various forward voltages.
4. The plot is drawn between the Forward voltage and Forward current.
   From the plot the forward resistance is calculated.

Table for Forward Bias:

S.No	Forward Voltage Vf (mV)	Forward Current If (mA)
1		
2		
3		
4		
5		
6		
7		
8		

MODEL GRAPH:

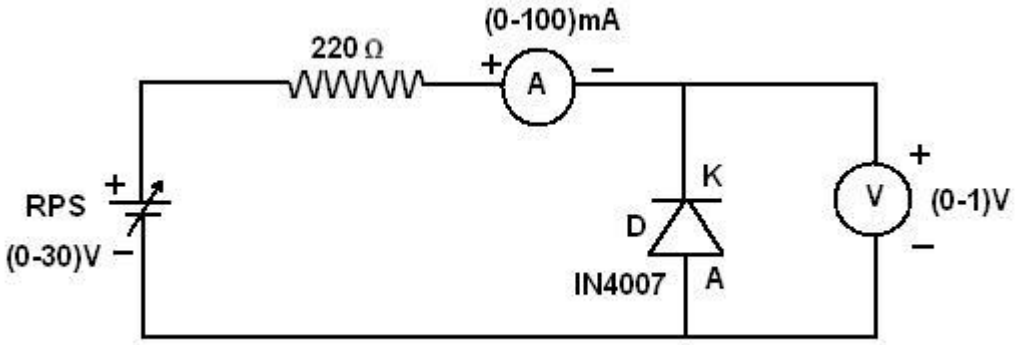


V-I Characteristics of a PN Diode

CALCULATION:

Forward resistance, $r_f = \frac{\text{Change in forward voltage}}{\text{Change in forward current}} = \frac{\Delta V_f}{\Delta I_f}$

REVERSE BIAS CHARACTERISTICS:



Circuit Diagram for Reverse Bias

PROCEDURE:

1. Connections are given as per the circuit diagram.
2. Power supply is switched ON.
3. By varying the RPS, the reverse current is noted for various reverse voltages.
4. The plot is drawn between the reverse voltage and reverse current.
5. From the plot the reverse resistance is calculated.

Table for Reverse Bias:

S.No	Reverse Voltage Vr (mV)	Reverse Current Ir (mA)
1		
2		
3		
4		
5		
6		
7		
8		

CALCULATION:

(i) Reverse resistance, $r_r = \frac{\text{Change in reverse voltage}}{\text{Change in reverse current}} = \frac{\Delta V_r}{\Delta I_r}$

RESULT:

Thus the V-I characteristics of a PN diode is drawn for both forward and reverse bias condition.

CHARACTERISTICS OF ZENER DIODE

EX. NO: 2

AIM:

To determine the forward and reverse characteristics of a zener diode.

APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1	RPS	(0-30)V	1
2	Resistor	220Ω	1
3	DC Voltmeter	(0-1)V	1
4	DC Ammeter	(0-100)mA	1
5	Zener Diode	IN4730	1
6	Bread board	-	1
7	Connecting wires	-	Few

THEORY:

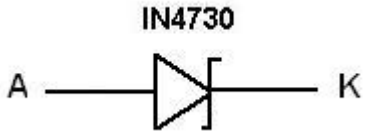
Zener diode is a special diode with increased amounts of doping. This is to compensate for the damage that occurs in the case of a *pn* junction diode when the reverse bias exceeds the breakdown voltage and thereby current increases at a rapid rate.

Applying a positive potential to the anode and a negative potential to the cathode of the zener diode establishes a forward bias condition. The forward characteristic of the zener diode is same as that of a *pn* junction diode i.e. as the applied potential increases the current increases exponentially. Applying a negative potential to the anode and positive potential to the cathode reverse biases the zener diode.

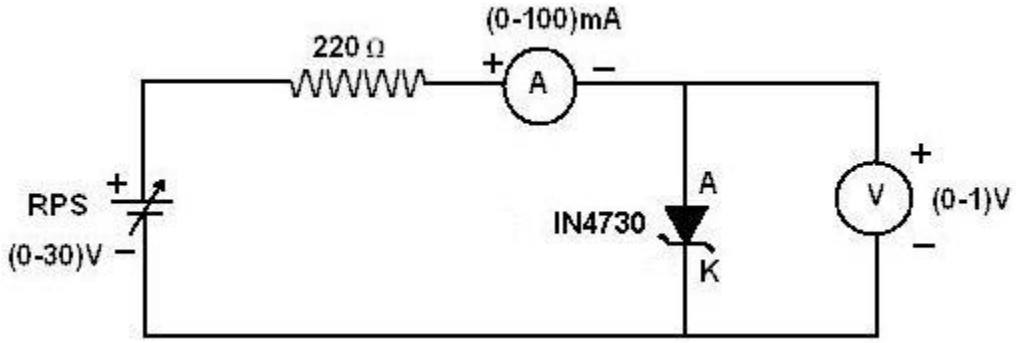
As the reverse bias increases the current increases rapidly in a direction opposite to that of the positive voltage region. Thus under reverse bias condition breakdown occurs. It occurs because there is a strong electric filed in the region

of the junction that can disrupt the bonding forces within the atom and generate carriers. The breakdown voltage depends upon the amount of doping. For a heavily doped diode depletion layer will be thin and breakdown occurs at low reverse voltage and the breakdown voltage is sharp. Whereas a lightly doped diode has a higher breakdown voltage. This explains the zener diode characteristics in the reverse bias region.

SYMBOL OF ZENER DIODE:



FORWARD BIAS CHARACTERISTICS:



Circuit Diagram for Forward Bias

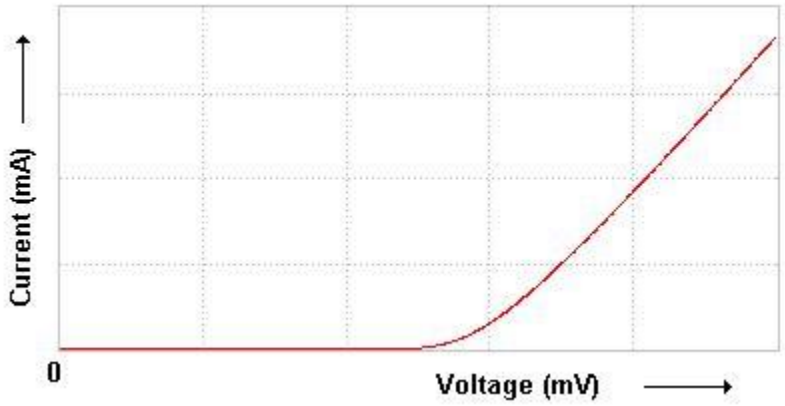
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. Power supply is switched ON.
3. By varying the RPS, the forward current is noted for various forward voltages.
4. The plot is drawn between the Forward voltage and Forward current.
5. From the plot the forward resistance is calculated.

Table for Forward Bias:

S.No	Forward Voltage Vf (mV)	Forward Current If (mA)
1		
2		
3		
4		
5		
6		
7		
8		

MODEL GRAPH:

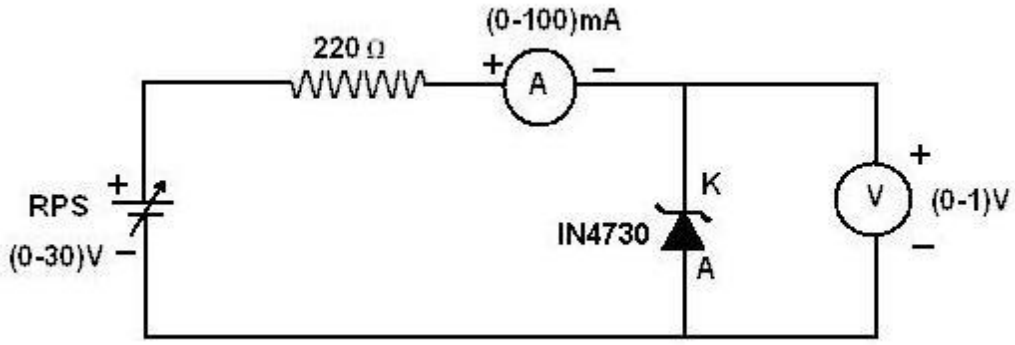


Forward Characteristics of a Zener Diode

CALCULATION:

Forward resistance, $r_f = \frac{\text{Change in forward voltage}}{\text{Change in forward current}} = \frac{\Delta V_f}{\Delta I_f}$

REVERSE BIAS CHARACTERISTICS:



Circuit Diagram for Reverse Bias

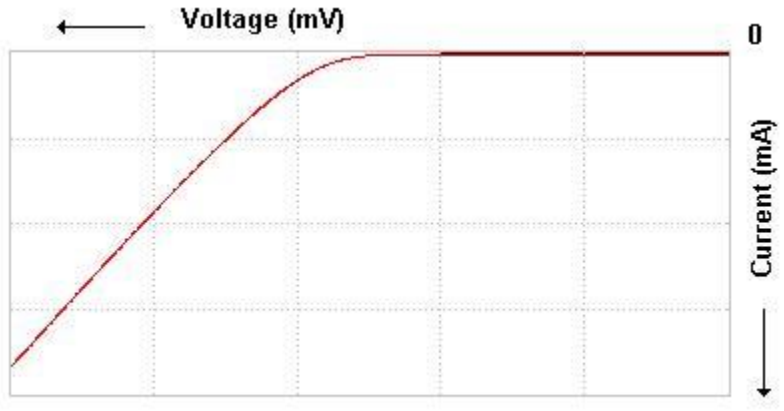
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. Power supply is switched ON.
3. By varying the RPS, the reverse current is noted for various reverse voltages.
4. The plot is drawn between the reverse voltage and reverse current.
5. From the plot the reverse resistance is calculated.

Table for Reverse Bias:

S.No	Reverse Voltage Vr (mV)	Reverse Current Ir (mA)
1		
2		
3		
4		
5		
6		
7		
8		

MODEL GRAPH:



Reverse Characteristics of a Zener Diode

CALCULATION:

Reverse resistance, $r_r = \frac{\text{Change in reverse voltage}}{\text{Change in reverse current}} = \frac{\Delta V_r}{\Delta I_r}$

RESULT:

Thus the V-I characteristics of a Zener diode is drawn for both forward and reverse bias condition.

CHARACTERISTICS OF BJT IN CE CONFIGURATION

EX. NO : 3

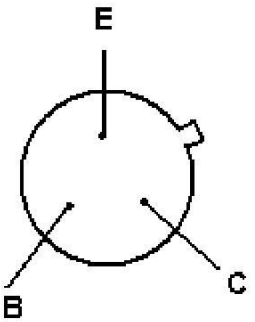
AIM:

To plot the input and output characteristics of a bipolar junction transistor (BJT) in common emitter (CE) configuration.

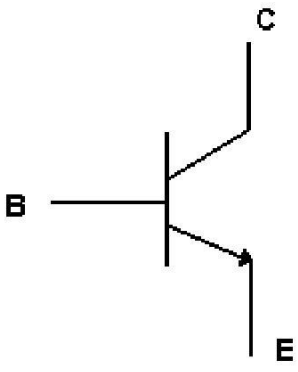
APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1	RPS	(0-30)V	2
2	Resistor	1KΩ	2
3	DC Voltmeter	(0-30)V	1
4	DC Voltmeter	(0-10)V	1
5	DC Ammeter	(0-50)μA	1
6	DC Ammeter	(0-30)mA	1
7	BJT	BC547	1
8	Bread board	-	1
9	Connecting wires	-	Few

THEORY:



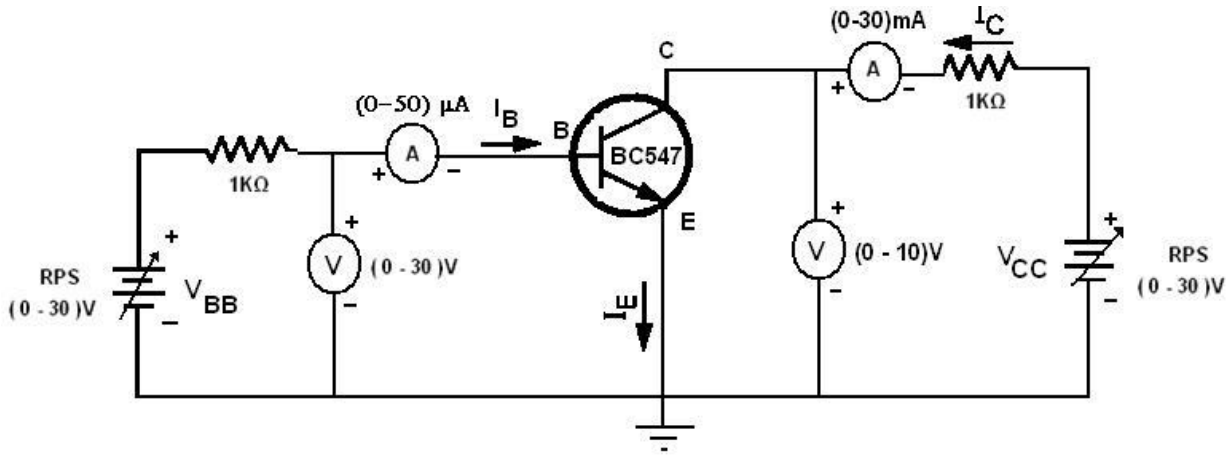
Pin Diagram of BJT



Symbol of BJT

The input is applied between emitter and base and output is taken from the collector and emitter. Here, emitter of the transistor is common to both input and output circuits and hence the name common emitter (CE) configuration.

Regardless of circuit configuration, the base emitter junction is always forward biased while the collector-base junction is always reverse biased, to operate transistor in active region.

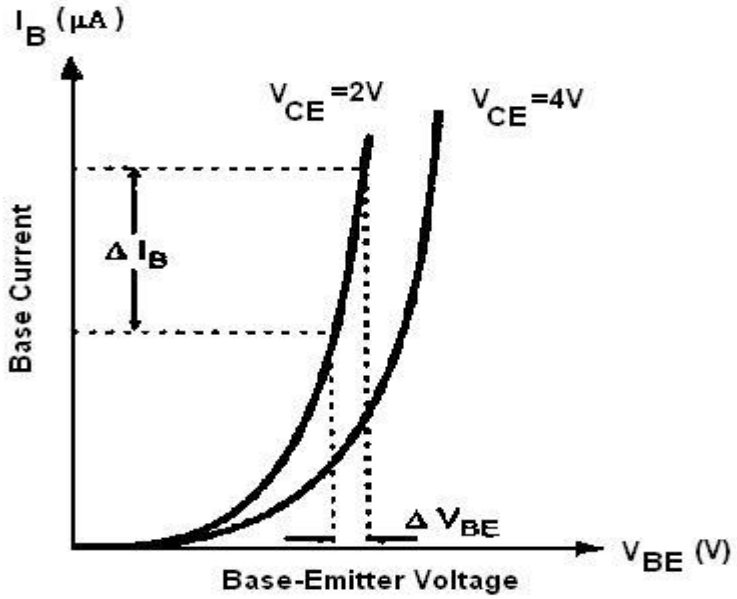


Circuit Diagram for a BJT in CE Configuration

INPUT CHARACTERISTICS:

PROCEDURE:

1. Connections are given as per the circuit diagram.
2. The supply is switched ON.
3. The collector-emitter voltage VCE is kept constant.
4. By varying the emitter-base voltage VBE, the various base current IB is noted.
5. The same procedure is repeated for various collector-emitter voltages VCE.
6. The input characteristic is the curve between input current IB and input voltage VBE at constant collector-emitter voltage VCE. The base current is taken along Y-axis and base-emitter voltage along X-axis.



Input Characteristics of a Transistor in CB Configuration

Table for Input Characteristics:

S.No	VCE = 2V		VCE = 4V	
	VBE(volts)	IB (μA)	VBE(volts)	IB (μA)
1				
2				
3				
4				
5				
6				
7				
8				

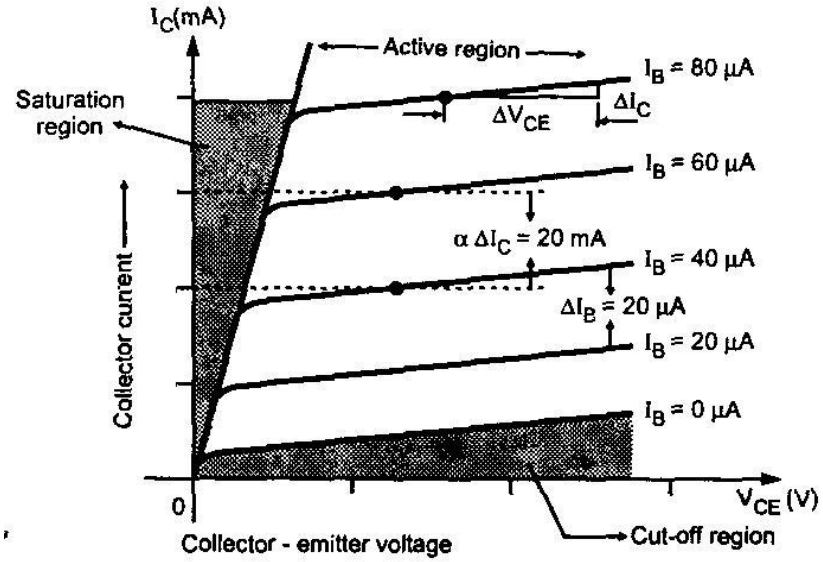
From this characteristic we observe the following important points.

1. As the input to a transistor in the CE configuration is between the base-to-emitter junctions, the CE input characteristics resembles a family of forward-biased diode curves.
2. After the cut-in voltage (barrier potential, normally 0.7 V for silicon and 0.3 V for Germanium), the base current (IB) increases rapidly with small increase in emitter-base voltage (VEB). It means that input resistance is very small. Because input resistance is a ratio of change in emitter-base voltage (ΔVEB) to the resulting changes in base current (ΔIB) at constant collector-emitter voltage (VCE), this resistance is also known as the dynamic input resistance of the transistor in CE configuration.
3. For a fixed value of VBE, IB decreases as VCE is increased. A larger value of VCE results in a large reverse bias at collector-base p-n junction. This increases the depletion region and reduces the effective width of the base. Hence, there are fewer recombinations in the base region, reducing the base current IB.

OUTPUT CHARACTERISTICS:

PROCEDURE:

1. Connections are given as per the circuit diagram.
2. The supply is switched ON.
3. The base current IB is kept constant.
4. By varying the collector-emitter voltage VCE, the various collector current IC is noted.
5. The same procedure is repeated for various base current IB.
6. The output characteristic is the curve between collector current IC and collector emitter voltage VCE at constant base current IB. The collector current is taken along Y-axis and collector-emitter voltage magnitude along X-axis.



Output Characteristics of a Transistor in CB Configuration

Table for Output Characteristics:

S.No	IB = 0 μA		IB = 20 μA		IB = 40 μA	
	VCE(volts)	IC (mA)	VCE(volts)	IC (mA)	VCE(volts)	IC (mA)
1						
2						
3						
4						
5						
6						
7						

From the output characteristics we can see that,

1. The change in collector-emitter voltage (ΔVCE) causes the little change in the collector current (ΔIC) for constant base current IB.
2. The output characteristic of common emitter configuration consists of three regions: Active, Saturation, and cut-off.
3. **Active region**: The region where the curves are approximately horizontal is the "active" region of the CE configuration. In the active region, the collector junction is reverse biased. As VCE is increased, reverse bias increases. This causes depletion region to spread more in base than in collector, reducing the chances of recombination in the base.
4. **Saturation region** : If VCE is reduced to a small value such as 0.2 V, then collector-base junction becomes forward biased, since the emitter base junction is already forward biased by 0.7 V. The input junction in CE configuration is base to emitter junction, which is always forward biased to operate transistor in active region. Thus input characteristics of CE configuration are similar to forward characteristics of p-n junction diode. When both the junctions are forward biased, the transistor operates in the saturation region, which is indicated on the output characteristics. The saturation value of VCE, designated VCE (sat) usually ranges between 0.1 V to 0.3 V.
5. **Cut-off region**: When the input base current is made equal to zero, the collector current is the reverse leakage current. Accordingly, in order to cut-off the transistor, it is not enough to reduce IB = 0. Instead, it is necessary to reverse bias the emitter junction slightly. We shall define cut-off as the condition where the collector current is equal to reverse saturation current and the emitter current is zero.

RESULT:

Thus the input and output characteristics of a bipolar junction transistor in common emitter configuration is analyzed.

CHARACTERISTICS OF BJT IN CB CONFIGURATION

EX. NO : 4

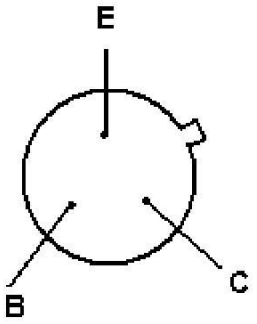
AIM:

To plot the input and output characteristics of a bipolar junction transistor (BJT) in common base (CB) configuration.

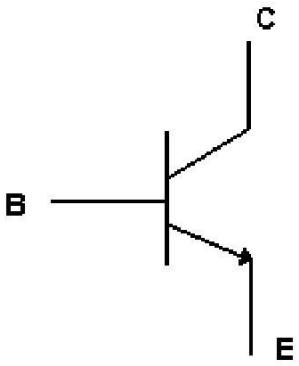
APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1	RPS	(0-30)V	2
2	Resistor	1KΩ	2
3	DC Voltmeter	(0-30)V	2
4	DC Ammeter	(0-10)mA	1
5	DC Ammeter	(0-30)mA	1
6	BJT	BC547	1
7	Bread board	-	1
8	Connecting wires	-	Few

THEORY:



Pin Diagram of BJT

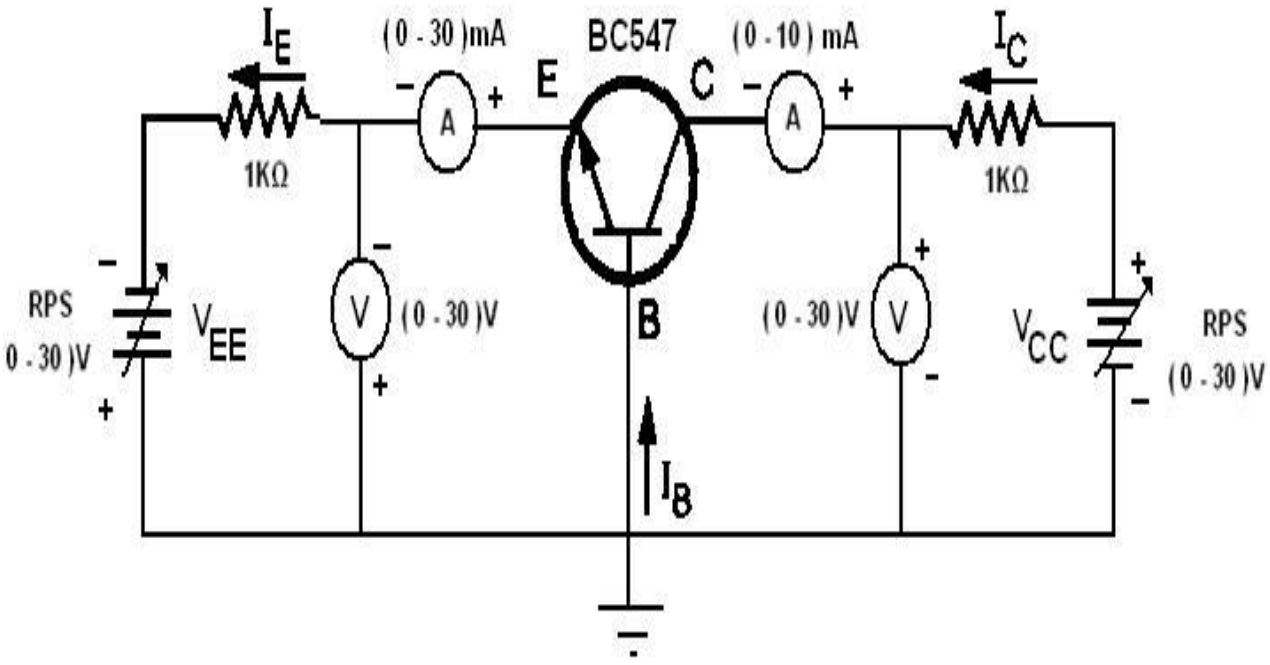


Symbol of BJT

The input is applied between emitter and base and output is taken from the collector and base. Here, base of the transistor is common to both input and output circuits and hence the name common base configuration.

Regardless of circuit configuration, the base emitter junction is always forward biased while the collector-base junction is always reverse biased, to operate transistor in active region.

Circuit Diagram for a BJT in CB Configuration



INPUT CHARACTERISTICS:

PROCEDURE:

1. Connections are given as per the circuit diagram.
2. The supply is switched ON.
3. The collector-base voltage VCB is kept constant.
4. By varying the emitter-base voltage VEB, the various emitter current IE is noted.
5. The same procedure is repeated for various collector-base voltages VCB.
6. The input characteristic is the curve between input current IE and input voltage VEB at constant collector-base voltage VCB. The emitter current is taken along Y-axis and emitter base voltage along X-axis

Input Characteristics of a Transistor in CB Configuration

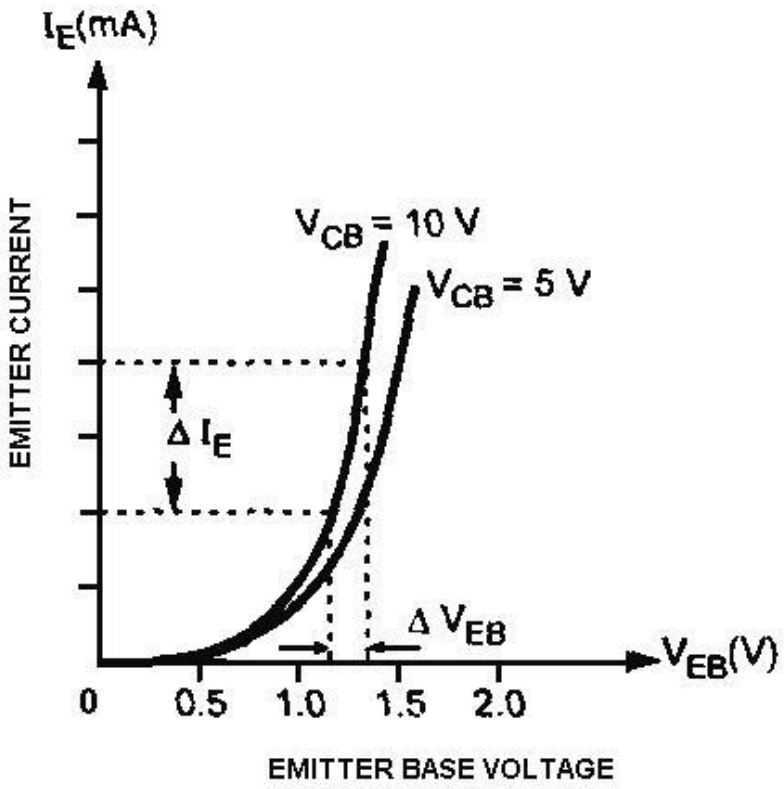


Table for Input Characteristics:

S.No	VCB = 5V		VCB = 10V	
	VEB(volts)	IE (mA)	VEB(volts)	IE (mA)
1				
2				
3				
4				
5				

From this characteristic we can observe the following important points

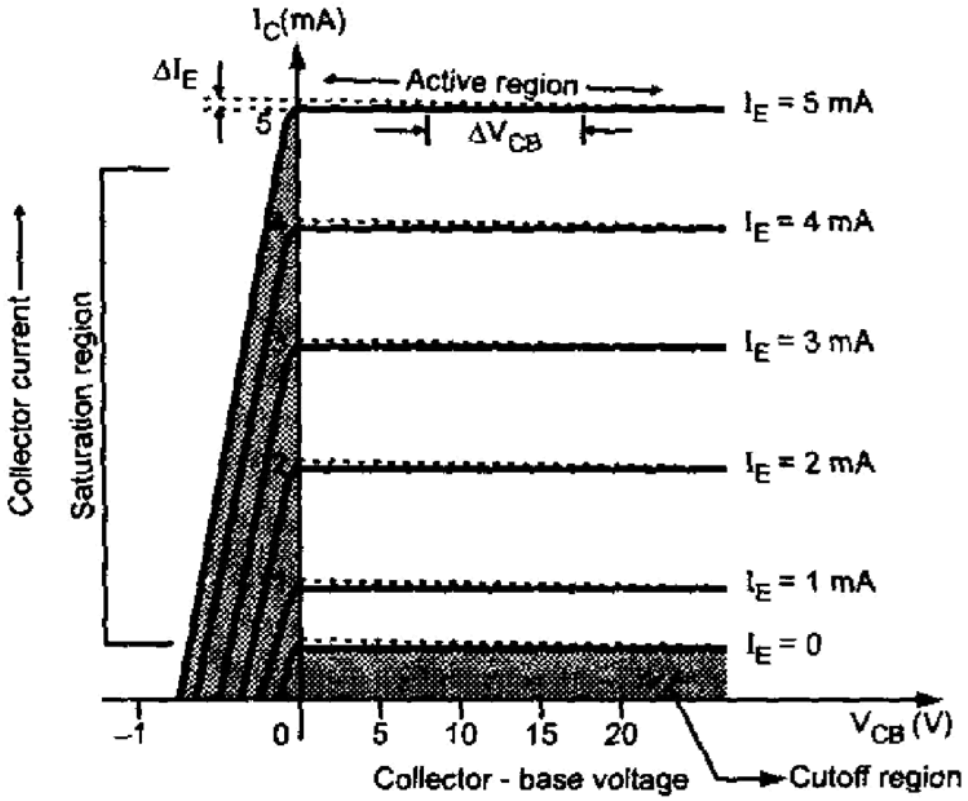
1. After the cut-in voltage (barrier potential, normally 0.7 V for silicon and 0.3 V for Germanium), the emitter current (IE) increases rapidly with small increase in emitter-base voltage (VEB). It means that input resistance is very small. Because input resistance is a ratio of change in emitter-base voltage (ΔVEB) to the resulting changes in emitter current (ΔIE) at constant collector-base voltage (VCB), this resistance is also known as the dynamic input resistance of the transistor in CB configuration.

2. It can be observed that there is slight increase in emitter current (IE) with increase in VCB. This is due to change in the width of the depletion region in the base region under the reverse biased condition.

OUTPUTCHARACTERISTICS:

PROCEDURE:

1. Connections are given as per the circuit diagram.
2. The supply is switched ON.
3. The emitter current IE is kept constant.
4. By varying the collector-base voltage VCB, the various collector current IC is noted.
5. The same procedure is repeated for various emitter current IE.
6. The output characteristic is the curve between collector current IC and collector base voltage VCB at constant emitter current IE. The collector current is taken along Y-axis and collector-base voltage magnitude along X-axis.



Output Characteristics of a Transistor in CB Configuration

Table for Output Characteristics:

S.No	IE = 0 mA		IE = 2 mA		IE = 4 mA	
	VBC(volts)	IC (mA)	VBC(volts)	IC (mA)	VBC(volts)	IC (mA)
1						
2						
3						
4						
5						

The output characteristic has three basic regions: Active, cut-off and saturation.

State	Emitter Base Junction	Collector Base Junction
Active	Forward Biased	Reverse Biased
Cut-off	Reverse Biased	Reverse Biased
Saturation	Forward Biased	Forward Biased

2. In active region, IC is approximately equal to IE and transistor works as an amplifier.
3. The region below the curve IE = 0 is called as cut-off region.
4. The saturation region is that region of the characteristics which is to the left of VCB =0 V. The exponential increase in collector current as the voltage VCB increases towards 0 V.
5. As IE increases IC also increases. Thus, IC depends upon input current IE but not on collector voltage. Hence, input current controls output current. Since transistor requires some current to drive it, it is called current operating device.

RESULT:

Thus the input and output characteristics of a bipolar junction transistor in common base configuration is analyzed.

JFET CHARACTERISTICS

EX NO:5A

AIM: a). To draw the drain and transfer characteristics of a given FET.

b). To find the drain resistance (r_d) amplification factor (μ) and Tran conductance (g_m) of the given FET.

APPARATUS:

S.NO	APPARATUS	RANGE	QUANTITY
1	RPS	(0-30)V	2
2	Resistor	1KΩ	2
3	DC Voltmeter	(0-20)V	1
4	DC Ammeter	(0-50)mA	1
5	JFET	BFW11	1
6	Bread board	-	1
7	Connecting wires	-	Few

THEORY:

A FET is a three terminal device, having the characteristics of high input impedance and less noise, the Gate to Source junction of the FET s always reverse biased. In response to small applied voltage from drain to source, the n-type bar acts as sample resistor, and the drain current increases linearly with $V_{DS.}$

With increase in I_D the ohmic voltage drop between the source and the channel region reverse biases the junction and the conducting position of the channel begins to remain constant.

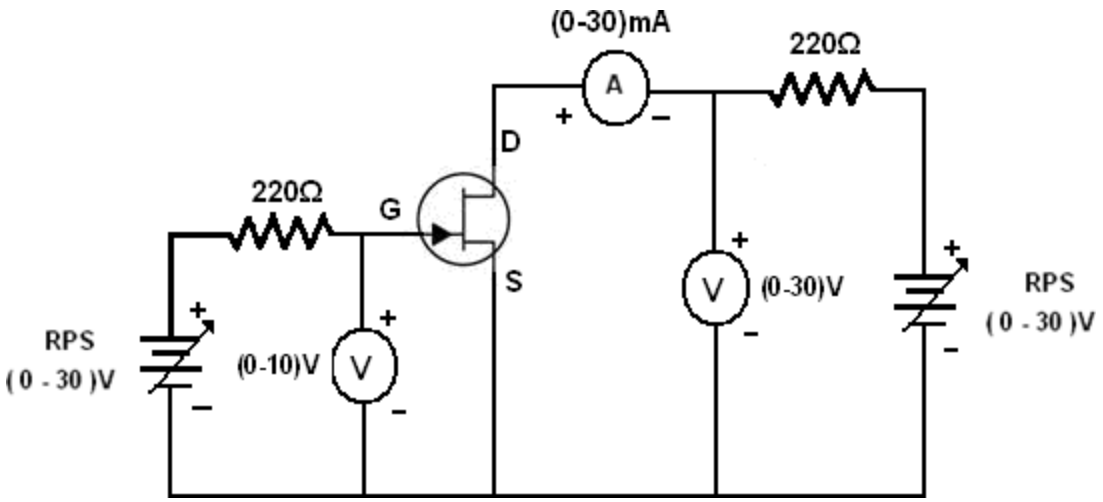
The V_{DS} at this instant is called “pinch of voltage”.

If the gate to source voltage (V_{GS}) is applied in the direction to provide additional reverse bias, the pinch off voltage ill is decreased.

In amplifier application, the FET is always used in the region beyond the pinch-off.

$F_{DS}=I_{DSS}(1-V_{GS}/V_P)\text{^}2$

CIRCUIT DIAGRAM



PROCEDURE:

1. All the connections are made as per the circuit diagram.
2. To plot the drain characteristics, keep V_{GS} constant at 0V.
3. Vary the V_{DD} and observe the values of V_{DS} and I_D.
4. Repeat the above steps 2, 3 for different values of V_{GS} at 0.1V and 0.2V.
5. All the readings are tabulated.
6. To plot the transfer characteristics, keep V_{DS} constant at 1V.
7. Vary V_{GG} and observe the values of V_{GS} and I_D.
8. Repeat steps 6 and 7 for different values of V_{DS} at 1.5 V and 2V.
9. The readings are tabulated.
10. From drain characteristics, calculate the values of dynamic resistance (r_d) by using the formula

    $r_d = \Delta V_{DS}/\Delta I_D$

11. From transfer characteristics, calculate the value of transconductace (g_m) By using the formula

    $G_m = \Delta I_D/\Delta V_{DS}$

12. Amplification factor (μ) = dynamic resistance. Tran conductance

    $\mu = \Delta V_{DS}/\Delta V_{GS}$

OBSERVATIONS:

DRAIN CHARACTERISTICS:

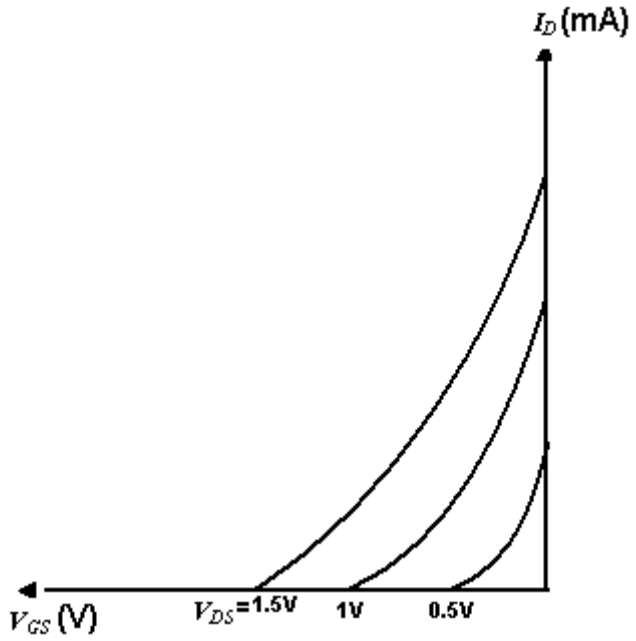
S.NO	V_{GS}=0V		V_{GS}= -1V		V_{GS}= -2V	
	V_{DS}(V)	I_D(mA)	V_{DS}(V)	I_D(mA)	V_{DS}(V)	I_D(mA)

TRANSFER CHARACTERISTICS:

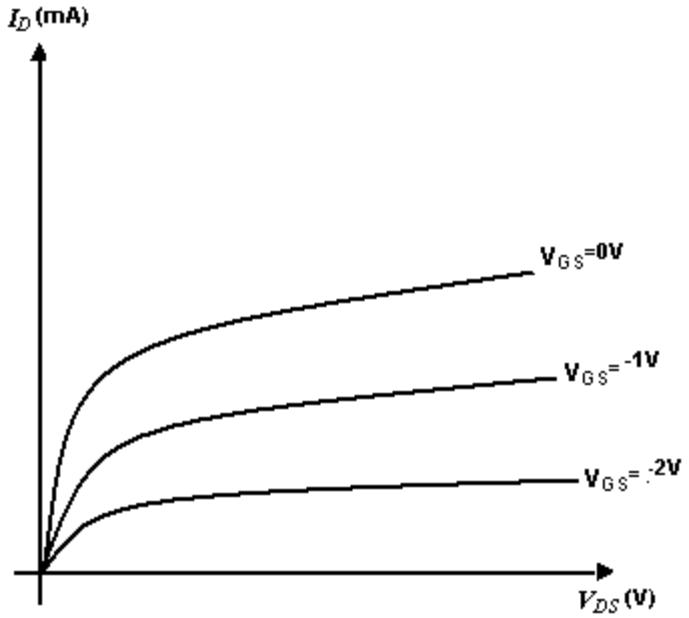
S.NO	V_{DS} =0.5V		V_{DS}=1V		V_{DS} =1.5V	
	V_{GS} (V)	I_D(mA)	V_{GS} (V)	I_D(mA)	V_{GS} (V)	I_D(mA)

MODEL GRAPH:

TRANSFER CHARACTERISTICS



DRAIN CHARACTERISTICS



PRECAUTIONS:

1. The three terminals of the FET must be care fully identified
2. Practically FET contains four terminals, which are called source, drain, Gate, substrate.
3. Source and case should be short circuited.
4. Voltages exceeding the ratings of the FET should not be applied.

RESULT :

The drain and transfer characteristics of a given FET are drawn**.**The dynamic resistance (r_d), amplification factor (μ) and Tran conductance (g_m) of the given FET are calculated.

CHARACTERISTICS OF MOSFET

EX. NO : 5B

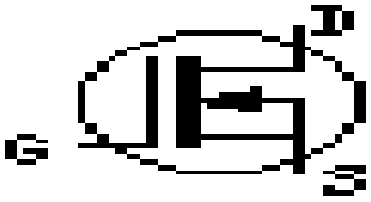
AIM:

To plot the drain and transfer characteristics of a n-channel depletion type Metal Oxide Semiconductor Junction Field Effect Transistor (MOSFET).

APPARATUS REQUIRED:

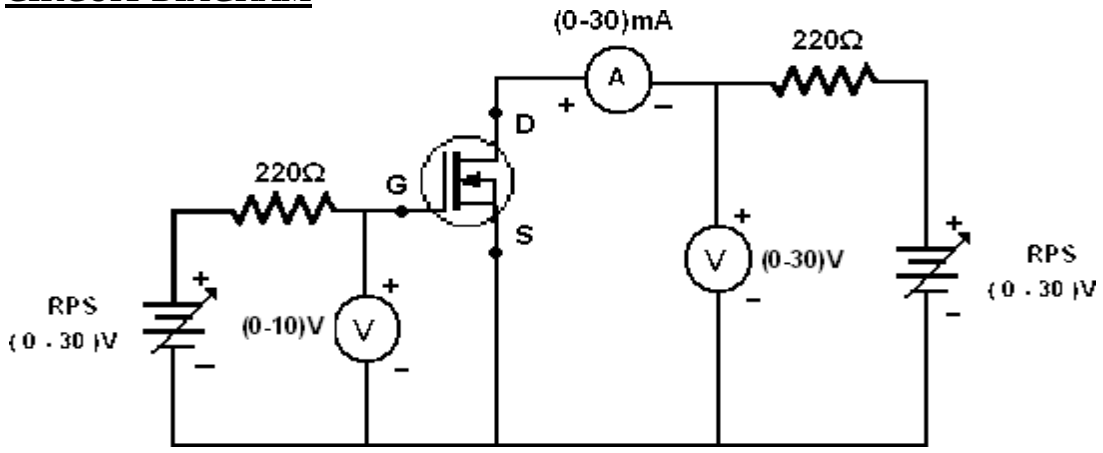
S.NO	APPARATUS	RANGE	QUANTITY
1	RPS	(0-30)V	2
2	Resistor	220Ω	2
3	DC Voltmeter	(0-10)V	1
4	DC Voltmeter	(0-30)V	1
5	DC Ammeter	(0-30)mA	1
6	MOSFET		1
7	Bread board	-	1
8	Connecting wires	-	Few

THEORY:



The metal–oxide–semiconductor field-effect transistor (MOSFET, MOS- FET, or MOS FET) is a device used to amplify or switch electronic signals. The MOSFET differs from JFET in that it has no p-n junction structure. Instead, the gate of the MOSFET insulated from the channel by a silicon dioxide (SiO_2) layer. Due to this the input resistance of MOSFET is greater than JFET.

CIRCUIT DIAGRAM



DRAIN CHARACTERICTICS:
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. The supply is switched ON.
3. The gate-source voltage V_{GS} is kept constant.
4. By varying the drain-source voltage V_{DS}, the various drain current I_D is noted.
5. The same procedure is repeated for various gate-source voltage V_{GS}

MODEL GRAPH:

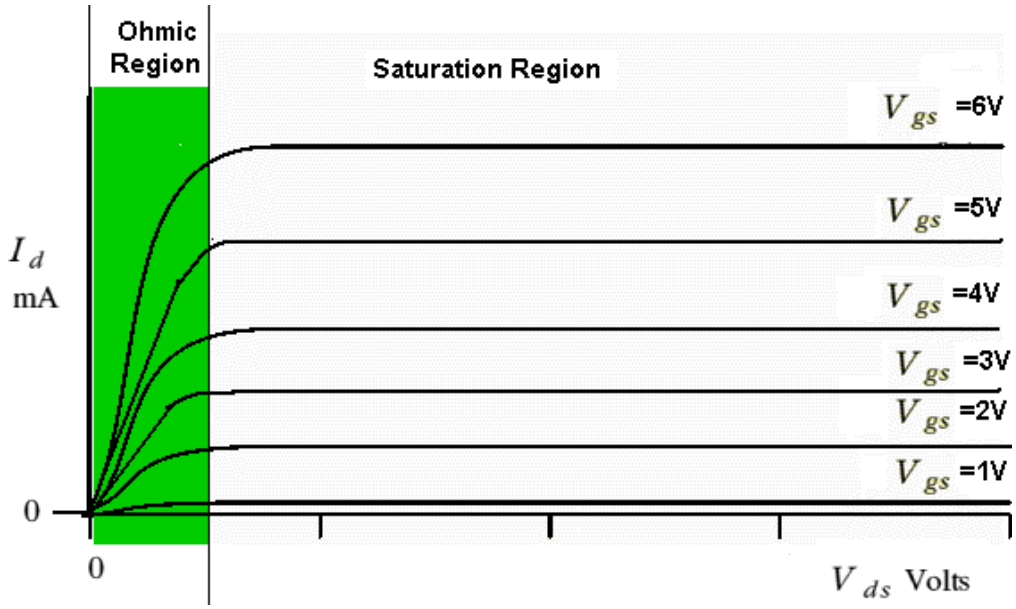


Table for Drain Characteristics:

S.No	V_{GS} =		V_{GS} =	
	I_D (mA)	V_{DS}(volts)	I_D (mA)	V_{DS}(volts)
1				
2				
3				
4				
5				
6				
7				

TRANSFER CHARACTERISTICS:

PROCEDURE:

1. Connections are given as per the circuit diagram.
2. The supply is switched ON.
3. The drain-source voltage V_{DS} is kept constant.
4. By varying the gate-source voltage $V_{GS,}$ the various drain current I_D is noted.
5. The same procedure is repeated for various drain-source voltage V_{DS}.

MODEL GRAPH:

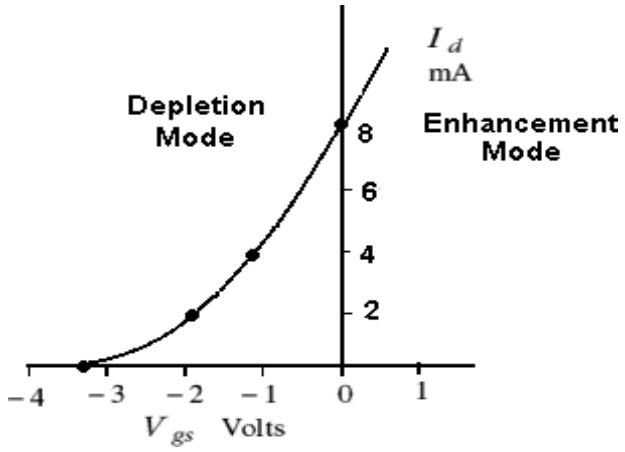
6. 

Table for Transfer Characteristics:

S.No	V_{DS} =		V_{DS} =	
	V_{GS}(volts)	I_D (mA)	V_{GS}(volts)	I_D (mA)
1				
2				
3				
4				
5				
6				
7				

RESULT:

Thus the drain and transfer characteristics of a metal oxide semiconductor junction field effect transistor is analyzed.

SILICON-CONTROLLED RECTIFIER(SCR) CHARACTERISTICS

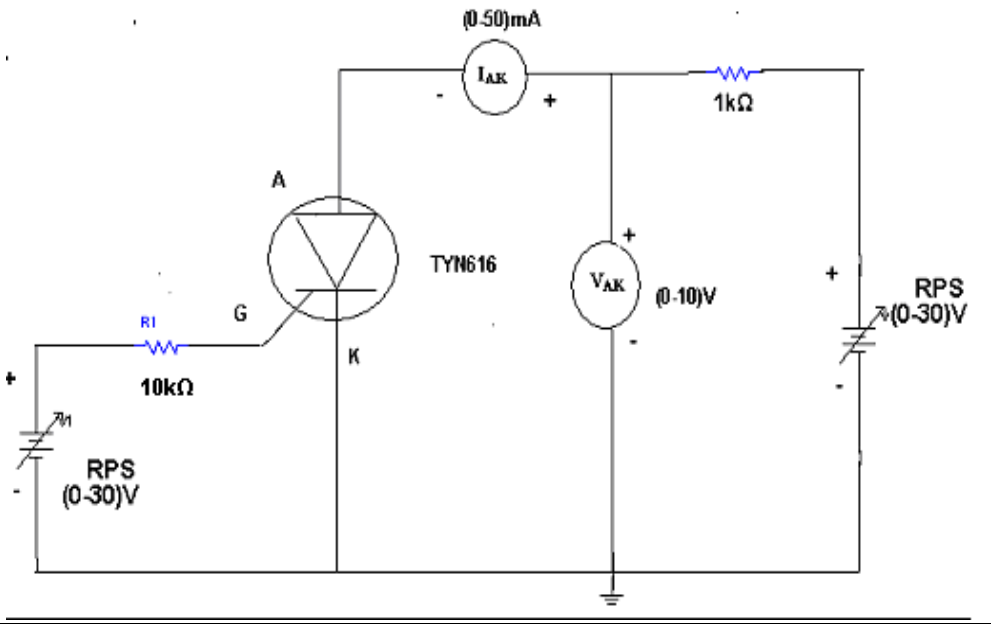
EX NO: 6

AIM: To draw the V-I Charateristics of SCR

APPARATUS:

S.NO	APPARATUS	RANGE	QUANTITY
1	RPS	(0-30)V	2
2	Resistor	1KΩ,10K	2
3	DC Voltmeter	(0-10)V	1
4	DC Ammeter	(0-30)mA	1
5	DC Ammeter	(0-50)mA	1
6	SCR	TY616	1
7	Bread board	-	1
8	Connecting wires	-	Few

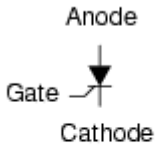
CIRCUIT DIAGRAM:



THEORY:

It is a four layer semiconductor device being alternate of P-type and N-type silicon. It consists os 3 junctions J_1, J_2, J_3 the J_1 and J_3 operate in forward direction and J_2 operates in reverse direction and three terminals

called anode A, cathode K , and a gate G. The operation of SCR can be studied when the gate is open and when the gate is positive with respect to cathode.



Schematic symbol

When gate is open, no voltage is applied at the gate due to reverse bias of the junction J_2 no current flows through R_2 and hence SCR is at cutt off. When anode voltage is increased J_2 tends to breakdown.

When the gate positive,with respect to cathode J_3 junction is forward biased and J_2 is reverse biased .Electrons from N-type material move across junction J_3 towards gate while holes from P-type material moves across junction J_3 towards cathode. So gate current starts flowing ,anode current increaase is in extremely small current junction J_2 break down and SCR conducts heavily.

When gate is open thee breakover voltage is determined on the minimum forward voltage at which SCR conducts heavily.Now most of the supply voltage appears across the load resistance.The holfing current is the maximum anode current gate being open , when break over occurs.

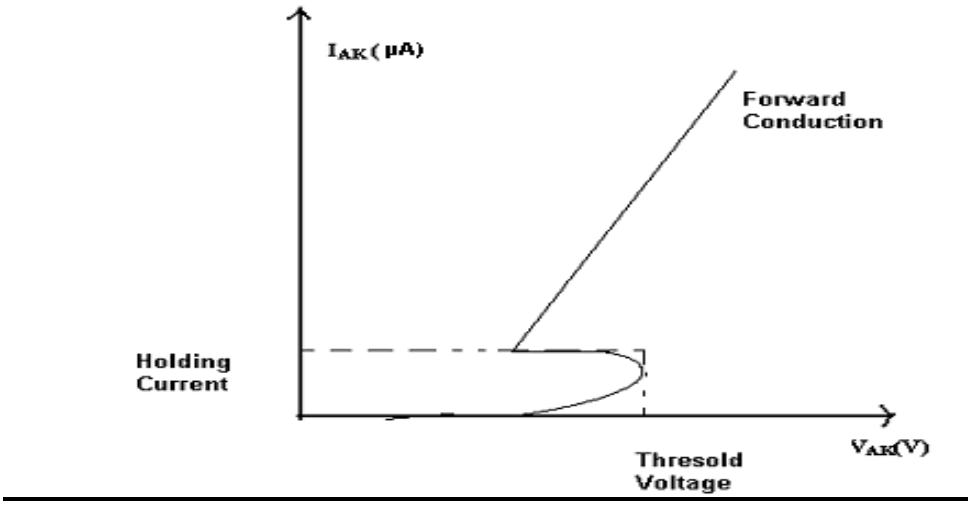
PROCEDURE:

1. Connections are made as per circuit diagram.
2. Keep the gate supply voltage at some constant value
3. Vary the anode to cathode supply voltage and note down the readings of voltmeter and ammeter.Keep the gate voltage at standard value.
4. A graph is drawn between V_{AK} and I_{AK} .

OBSERVATION

V_{AK}(V)	**I_{AK} (µA)**

MODEL WAVEFORM:



RESULT: \

SCR Characteristics are observed and plotted.

CHARACTERISTICS OF CLIPPERS

EX NO:7A

AIM:

To construct and study the operation of clipper circuits.

APPARATUS REQUIRED:

S.No	COMPONENTS	RANGE/SPECIFICATION	QUANTITY
1.	Resistor	10KΩ	1each
2.	CRO	(0-20)MHZ	1
3.	Diode	IN4001	1
4.	Bread Board		1
5.	Regulated power Supply	(0 – 30)V	1

THEORY:

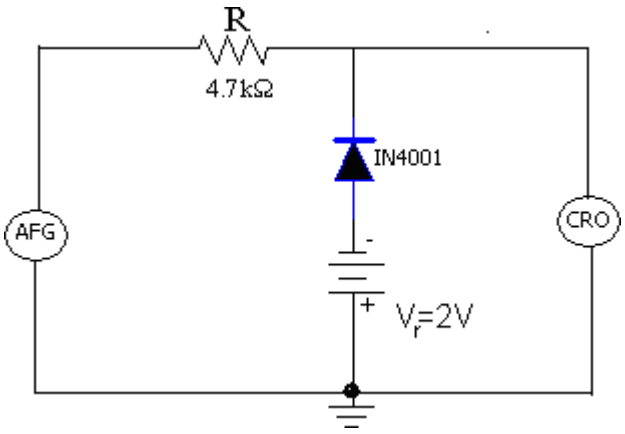
The basic action of a clipper circuit is to remove certain portions of the waveform, above or below certain levels as per the requirements. Thus the circuits which are used to clip off unwanted portion of the waveform, without distorting the remaining part of the waveform are called clipper circuits or Clippers. The half wave rectifier is the best and simplest type of clipper circuit which clips off the positive/negative portion of the input signal. The clipper circuits are also called limiters or slicers.

PROCEDURE

Clipper Circuit

1. Connect the components and apparatus as shown in the circuit diagram.
2. Set input, sinusoidal signal of 8Vp-p and 1 kHz frequency and the reference voltage as 2V using RPS.
3. Observe the output across the diode using CRO.Plot the input and output signal in a linear graph.

NEGATIVE PEAK CLIPPER



MODEL GRAPH

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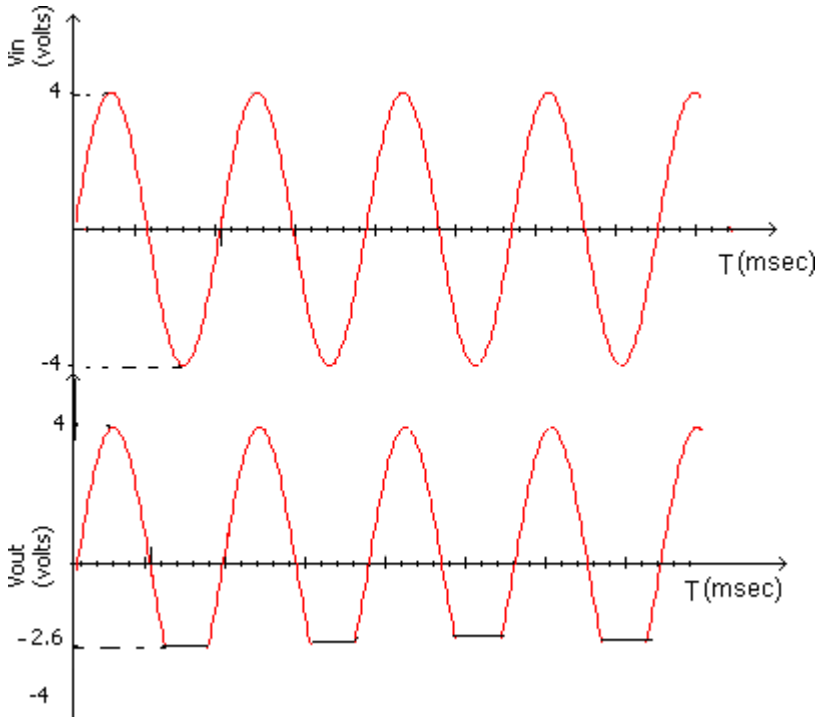


Theoretical calculations:

Vr=2v, Vγ=0.6v
When the diode is forward biased Vo =-(Vr+ Vγ) = -(2v+0.6v)= -2.6v When the diode isreverse biased the Vo=Vi

TABULATION FOR NEGATIVE CLIPPER:

S.NO	INPUT		OUTPUT	
	TIME	AMPLITUDE	TIME	AMPLITUDE

TABULATION FOR POSITIVE CLIPPER:

S.NO	INPUT		OUTPUT	
	TIME	AMPLITUDE	TIME	AMPLITUDE

RESULT:

Thus the clipper circuits are designed and the output waveforms are observed.

CLAMPER CIRCUIT

EX NO:7B

AIM:

To construct and study the output waveforms of clamper circuits.

APPARATUS REQUIRED:

S.No	COMPONENTS	RANGE/SPECIFICATION	QUANTITY
1.	CRO	(0-30)MHZ	1each
2.	Capacitor	1000µf/25V	1
3.	Diode	IN4001	1
4.	Bread Board		1
5.	Regulated power supply	(0 – 30)V	1

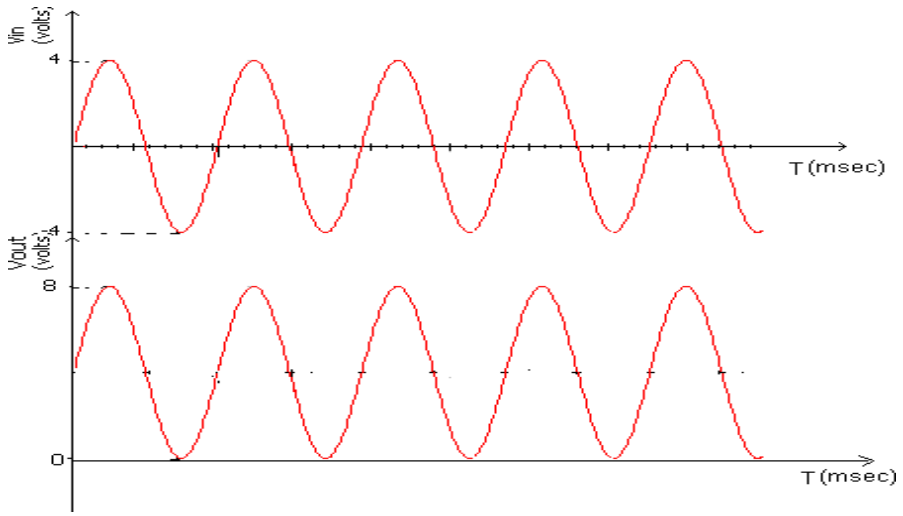
PROCEDURE

Clamper Circuit

1. Connect the components and apparatus as shown in the circuit diagram.
2. Set input, sinusoidal signal of 8Vp-p and 1kHz frequency
3. Observe the output across the load resistance using CRO.
4. Plot the input and output signal in a linear graph.

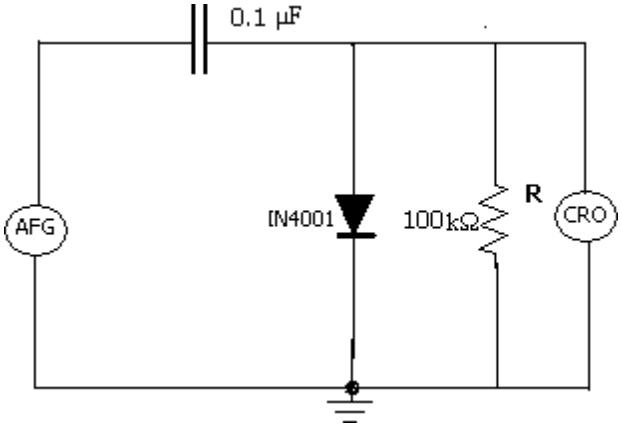
CIRCUIT DIAGRAM

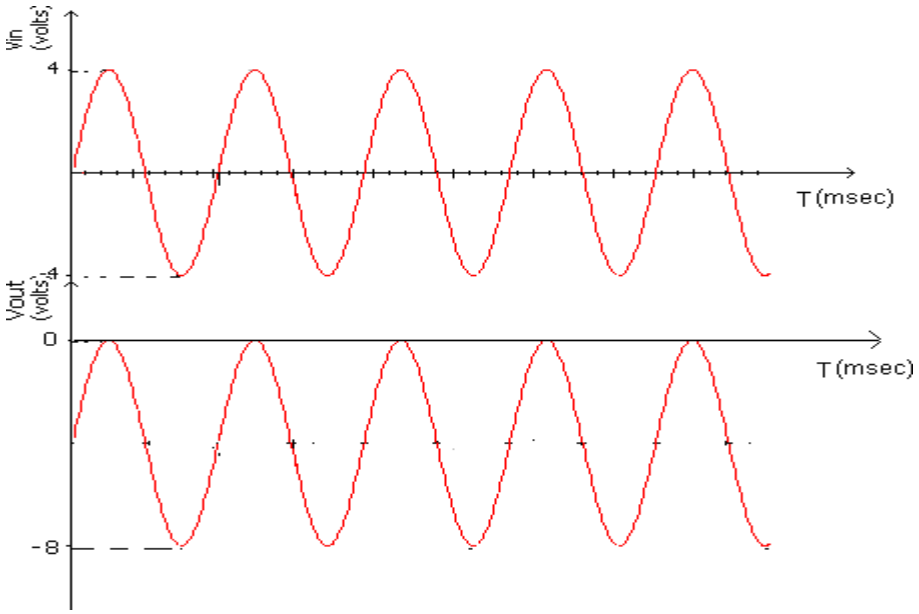
POSITIVE CLAMPER



CIRCUIT DIAGRAM

NEGATIVECLAMPER





TABULATION FOR POSITIVE CLAMPER:

S.NO	INPUT		OUTPUT	
	TIME	AMPLITUDE	TIME	AMPLITUDE

RESULT:

Thus the clamper circuits are designed and the output waveforms are observed.

FULL-WAVE RECTIFIER

EX NO:7C

AIM:-To find the Ripple factor and regulation of a Full-wave Rectifier with and without filter.

APPARATUS:- Experimental Board

Transformer (6-0-6v).

P-n Diodes, (lN4007) ---2 No's

Multimeters –2No's

Filter Capacitor (100μF/25v) -

Connecting Wires

Load resistor, 1KΩ

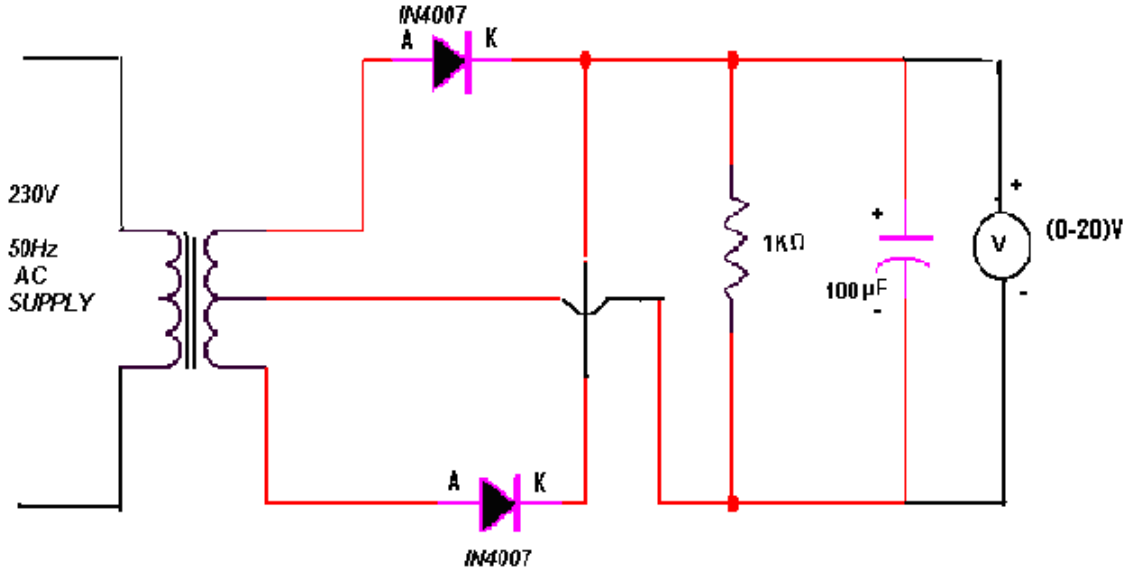
THEORY:-

The circuit of a center-tapped full wave rectifier uses two diodes D1&D2. During positive half cycle of secondary voltage (input voltage), the diode D1 is forward biased and D2is reverse biased.

The diode D1 conducts and current flows through load resistor R_L. During negative half cycle, diode

D2 becomes forward biased and D1 reverse biased. Now, D2 conducts and current flows through the load resistor R_L in the same direction. There is a continuous current flow through the load resistor R_L, during both the half cycles and will get unidirectional current as show in the model graph. The difference between full wave and half wave rectification is that a full wave rectifier allows unidirectional (one way) current to the load during the entire 360 degrees of the input signal and half-wave rectifier allows this only during one half cycle (180 degree).

CIRCUIT DIAGRAM:-



PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Connect the ac mains to the primary side of the transformer and the secondary side to the rectifier.
3. Measure the ac voltage at the input side of the rectifier.
4. Measure both ac and dc voltages at the output side the rectifier.
5. Find the theoretical value of the dc voltage by using the formula Vdc=2Vm/Π
6. Connect the filter capacitor across the load resistor and measure the values of Vac and Vdc at the output.
7. The theoretical values of Ripple factors with and without capacitor are calculated.
8. From the values of Vac and Vdc practical values of Ripple factors are calculated. The practical values are compared with theoretical values.

THEORITICAL CALCULATIONS:-

$$Vrms = Vm/\sqrt{2}$$

$$Vm = Vrms\sqrt{2}$$

$$Vdc = 2Vm/\Pi$$

(i)Without filter:

$$\text{Ripple factor, } r = \sqrt{(Vrms/Vdc)^2 - 1} = 0.482$$

(ii)With filter:

Ripple factor, $r = 1/ (4\sqrt{3}\ f\ C\ R_L)$ where f =50Hz

C =100μF

R_L=1KΩ

PRACTICAL CALCULATIONS:

Without filter:- Vac=

Vdc=

Ripple factor, r=Vac/Vdc

With filters:- Vac=

Vdc=

Ripple factor=Vac/Vdc

Without Filter

$V_{rms} = V_m/ \sqrt{2}$, $V_{dc}=2V_m/\Pi$, $V_{ac}=\sqrt{(V_{rms}^2 - V_{dc}^2)}$

S.NO	RL(OHM)	V_m(v)	V_{RMS}(v)	V_{dc}(v)	I_{DC} =Vdc/RL	r=V_{ac}/ V_{dc}

With Filter:

S.NO	RL(OHM)	V_m(v)	V_{RMS}(v)	V_{dc}(v)	I_{DC} =Vdc/RL	r=V_{ac}/ V_{dc}

PRECAUTIONS:

1. The primary and secondary side of the transformer should be carefully identified
2. The polarities of all the diodes should be carefully identified.

RESULT:-

The ripple factor of the Full-wave rectifier (with filter and without filter) is calculated.

THEVENIN'S THEOREM

EX. NO: 8(a)

AIM:

To verify the Thevenin's theorem for the given circuit.

APPARATUS REQUIRED:

S.NO	APPARATUS	TYPE	RANGE	QUANTITY
1	RPS	DC	(0-30)V	1
2	Resistor	-	1KΩ	3
3	Ammeter	DC	(0-10)mA	1
4	Bread board	-	-	1
5	Connecting wires	-	-	Few

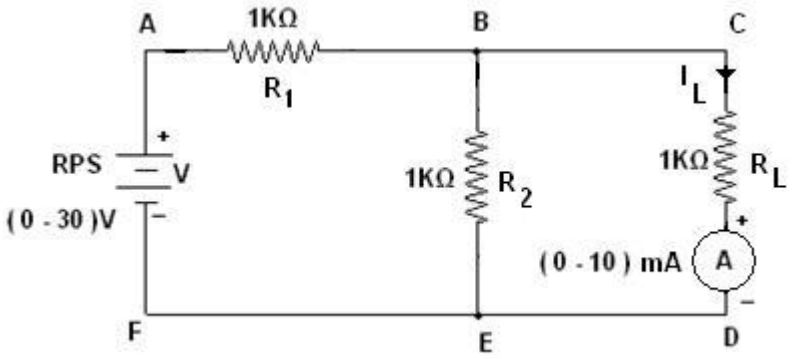
THEORY:

THEVENIN'S THEOREM:

Any linear active network with output terminals C and D can be replaced by a single voltage source (VTh = VOc) in series with a single impedance (ZTh = Zi).

VTh is the Thevenin's voltage. It is the voltage between the terminals C and D on open circuit condition. Hence it is called open circuit voltage denoted by VOc.

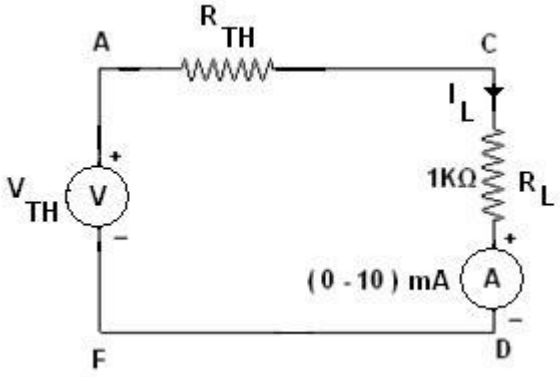
ZTh is called Thevenin's impedance. It is the driving point impedance at the terminals C and D when all the internal sources are set to zero. In case of DC ZTh is replaced by RTh.



Circuit Diagram for Thevenin's Theorem

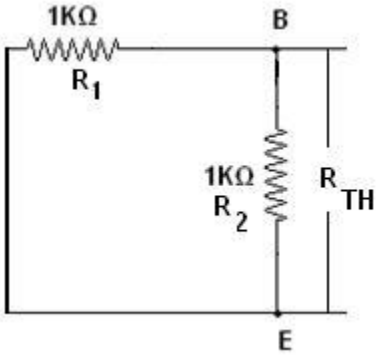
CALCULATION:

The Thevenin's equivalent circuit is,



$$I_L = \frac{V_{TH}}{R_{TH} + R_L}$$

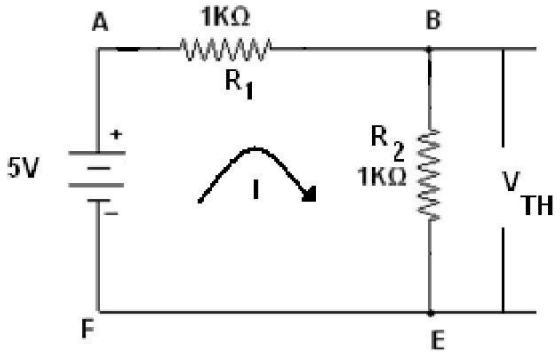
To Find RTH:



R_1 = 1K Ω ; R_2 = 1K Ω;

RTH= $\frac{R1*R2}{R1+R2}$

To Find VTH:



$$I = \frac{V}{R_T}$$

Let V = 5V,

VTH=VBE

$$\therefore I_L = \frac{V_{TH}}{R_{TH} + R_L}$$

PROCEDURE:

1. The circuit connections are given as per the circuit diagram.
2. Switch ON the power supply.
3. Initially set 5V as input voltage from RPS.
4. The ammeter reading is noted and the value is tabulated.

Table:

Let V = 5V

S .NO	Voltage in Volts	Load Current in Amps	
		Theoretical Value	Practical Value

RESULT:

Thus the Thevenin's theorem for the given circuit is verified successfully.

NORTON'S THEOREM

EX. NO: 8(b)

AIM:

To verify the Norton's theorem for the given circuit.

APPARATUS REQUIRED:

S.NO	APPARATUS	TYPE	RANGE	QUANTITY
1	RPS	DC	(0-30)V	1
2	Resistor	-	1KΩ	3
3	Ammeter	DC	(0-10)mA	1
4	Bread board	-	-	1
5	Connecting wires	-	-	Few

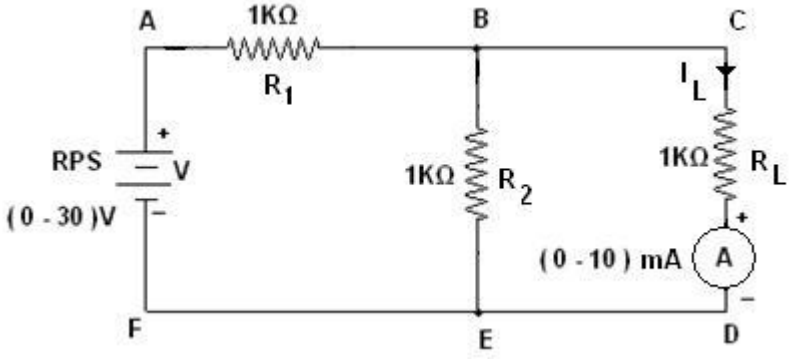
THEORY:

NORTON'S THEOREM:

Any linear active network with output terminals C and D can be replaced by a single current source ISC(IN) in parallel with a single impedance (ZTh = Zn).

ISC is the current through the terminals C and D on short circuit condition. ZTh is called Thevenin's impedance. In case of DC ZTh is replaced by RTh.

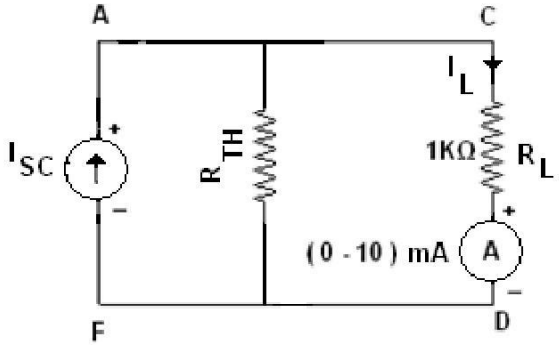
The current through impedance connected to the terminals of the Norton's equivalent circuit must have the same direction as the current through the same impedance connected to the original active network.



Circuit Diagram for Norton's Theorem

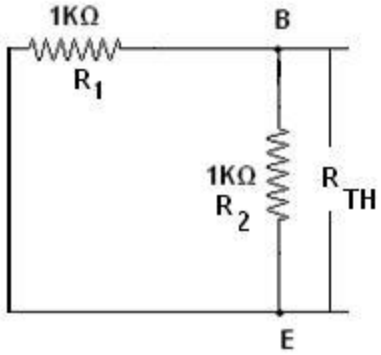
CALCULATION:

The Norton's equivalent circuit is,



$$I_L = \frac{I_{SC} R_{TH}}{R_{TH} + R_L}$$

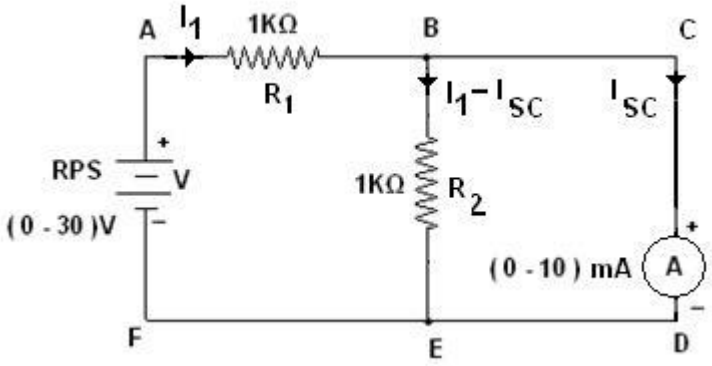
To Find RTH:



R_1 = 1K Ω ; R_2 = 1K Ω;

RTH= R1*R2
R1+R2

To Find ISC:



Let V=5V

In the loop ABEFA by applying KVL,

$I_1R_1 + (I_1 - I_{SC})R_2 = V$

$I_1 X\ 1 + (I_1 - I_{SC}) X\ 1 = 5$

$2I_1 - I_{SC} = 5 - - - - - - - - - - - - - - (1)$

In the loop BCDEB by applying KVL,

$(I_1 - I_{SC})R_2 = V$

$(I_1 - I_{SC}) X\ 1 = 0$

$I_1 - I_{SC} = 0 - - - - - - - - - - - - - - (2)$

From the equation (I) and (2),

$\therefore I_{SC} = 5\ mA$

$I_1 = 5\ mA$

IL = ISC*RTH
RTH+RL

PROCEDURE:

1. The circuit connections are given as per the circuit diagram.
2. Switch ON the power supply.
3. Initially set 5V as input voltage from RPS.
4. The ammeter reading is noted and the value is tabulated.

RESULT:

Thus the Norton's theorem for the given circuit is verified successfully.

KIRCHOFF'S VOLTAGE LAW

EX. NO: 9(a)

AIM:

To verify the Kirchoff's Voltage Law (KVL) for the given circuit.

APPARATUS REQUIRED:

S.NO	APPARATUS	TYPE	RANGE	QUANTITY
1	RPS	DC	(0-30)V	1
2	Resistor	-	1KΩ	3
3	Voltmeter	DC	(0-10)V	3
4	Bread board	-	-	1
5	Connecting wires	-	-	Few

FORMULA USED:

1. **CURRENT DIVISION RULE:**

$$I = \frac{\text{TOTAL CURRENT X OPPOSITE RESISTANCE}}{\text{TOTAL RESISTANCE}}$$

2. **OHM'S LAW:**

$$V=IR$$

Where, V = Voltage in Volts

I = Current in Amperes

R = Resister in Ohms

THEORY:

KIRCHOFF'S VOLTAGE LAW:

It states that the algebraic sum of all the voltages in a closed loop is equal to zero.

$$\sum V = 0$$

CALCULATION:

R_1 = **1K**Ω ; R_2 = **1K**Ω; R_3 = **1K**Ω

$$R_T = R_3 + R_p$$

$$= R_3 + \frac{R_1 R_2}{R_1 + R_2}$$

$$I = \frac{V}{R_T}$$

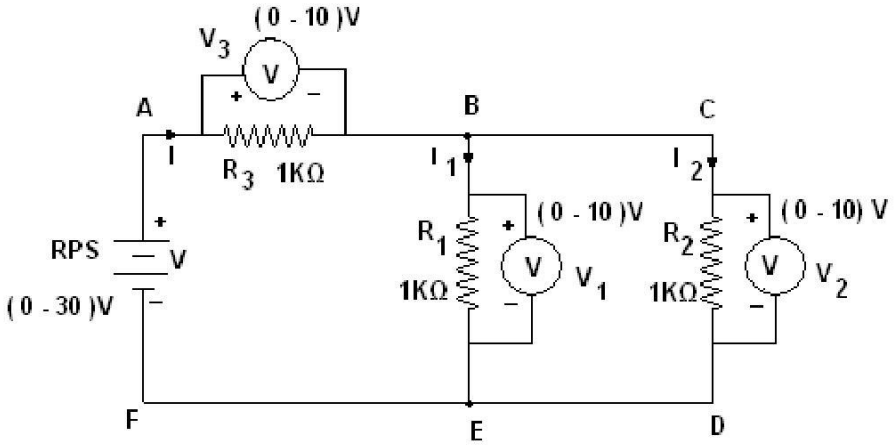
Let V = 5V,

I1= I*R2
R1+R2

V1=I1*R1

In the loop ABEFA,

$$V = V_3 + V_1$$



Circuit Diagram for Kirchoff's Voltage Law

PROCEDURE:

KIRCHOFF'S VOLTAGE LAW:

1. The circuit connections are given as per the circuit diagram.
2. Switch ON the power supply.
3. Initially set 5V as input voltage from RPS.
4. The voltmeter readings are noted and the values are tabulated.
5. The same procedure is repeated for various values.

Table:

Let V = 5V

S.NO	Applied voltage	Voltage in Volts		
		V1	V2	V3

RESULT:

Thus the Kirchoff's Voltage Law (KVL) for the given circuit is verified.

KIRCHOFF'S CURRENT LAW

EX. NO: 9(b)

AIM:

To verify the Kirchoff's Current Law (KCL) for the given circuit.

APPARATUS REQUIRED:

S.NO	APPARATUS	TYPE	RANGE	QUANTITY
1	RPS	DC	(0-30)V	1
2	Resistor	-	1KΩ	3
3	Ammeter	DC	(0-30)mA	3
4	Bread board	-	-	1
5	Connecting wires	-	-	Few

FORMULA USED:

1. CURRENT DIVISION RULE:

$$I = \frac{\text{TOTAL CURRENT X OPPOSITE RESISTANCE}}{\text{TOTAL RESISTANCE}}$$

2. OHM'S LAW:

$$V = IR$$

Where, V = Voltage in Volts

I = Current in Amperes

R = Resister in Ohms

THEORY:

KIRCHOFF'S CURRENT LAW:

It states that the algebraic sum of the currents meeting at a node is equal to zero.

$$\sum Current\ flow\ towards\ the\ node = \sum Current\ flow\ away\ from\ the\ node$$

CALCULATION:

R_1 = **1K**Ω ; R_2 = **1K**Ω; R_3 = **1K**Ω

$R_T = R_3 + R_P$

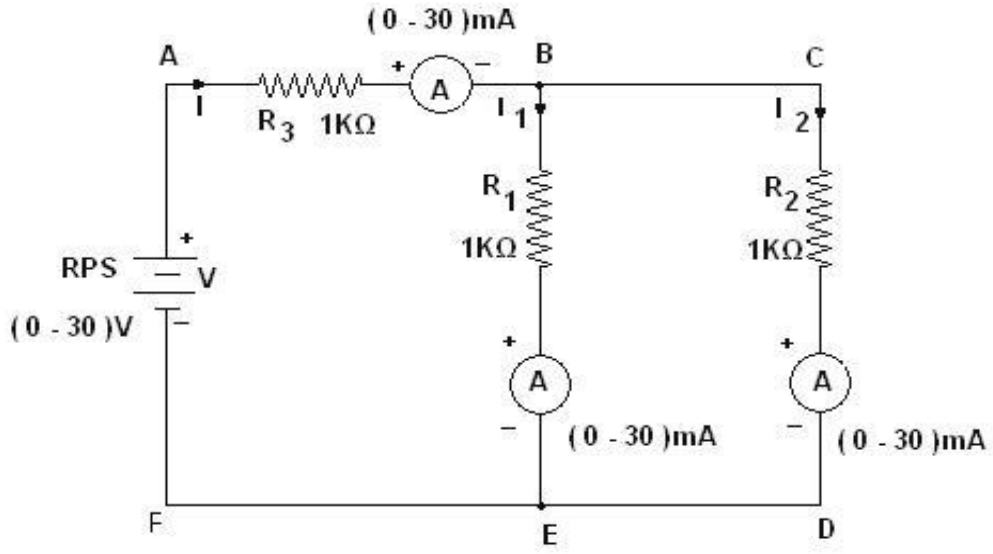
$$= R_3 + \frac{R_1 R_2}{R_1 + R_2}$$

$$I = \frac{V}{R_T}$$

Let V = 5V,

I1= I*R2
R1+R2

At node B the current = I=I1+I2



Circuit Diagram for Kirchoff's Current Law

PROCEDURE:

KIRCHOFF'S CURRENT LAW:

1. The circuit connections are given as per the circuit diagram.
2. Switch ON the power supply.
3. Initially set 5V as input voltage from RPS.
4. The ammeter readings are noted and the values are tabulated.
5. The same procedure is repeated for various values.

Table:

S.NO	Applied voltage	Current in amps		
		I1	I2	I=I1+I2

RESULT:

Thus the Kirchoff's Current Law (KCL) for the given circuit is verified.

SUPERPOSITION THEOREM

EX. NO: 10

AIM:

To verify the superposition theorem for the given circuit.

APPARATUS REQUIRED:

S.NO	APPARATUS	TYPE	RANGE	QUANTITY
1	RPS	DC	(0-30)V	2
2	Resistor	-	1KΩ,2K,10 K	3
3	Ammeter	DC	(0-50)mA	1
4	Bread board	-	-	1
5	Connecting wires	-	-	Few

THEORY:

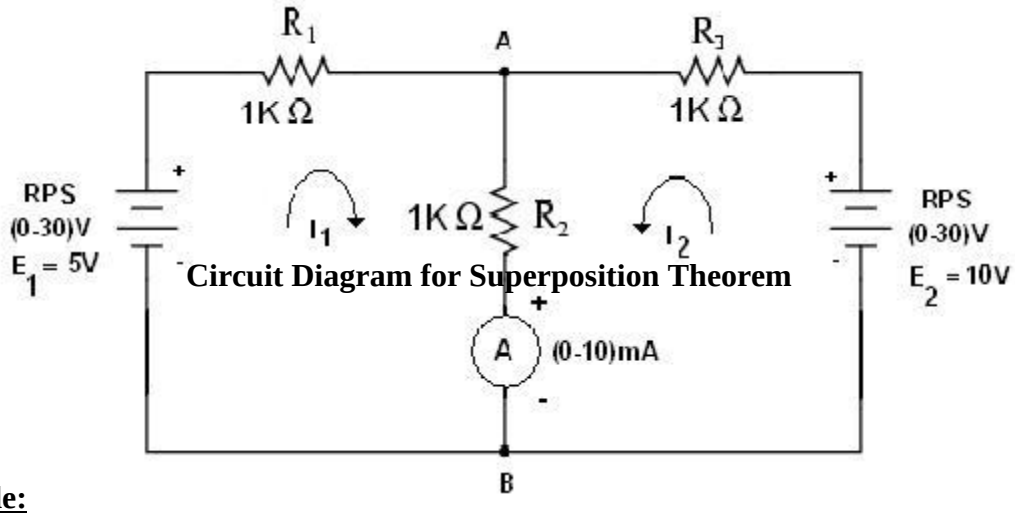
SUPERPOSITION THEOREM:

The superposition theorem for electrical circuits states that the total current in any branch of a bilateral linear circuit equals the algebraic sum of the currents produced by each source acting separately throughout the circuit.

To ascertain the contribution of each individual source, all of the other sources first must be "killed" (set to zero) by:

1. replacing all other voltage sources with a short circuit (thereby eliminating difference of potential. i.e. V=0)
2. replacing all other current sources with an open circuit (thereby eliminating current. i.e. I=0)

This procedure is followed for each source in turn, and then the resultant currents are added to determine the true operation of the circuit. The resultant circuit operation is the superposition of the various voltage and current sources.

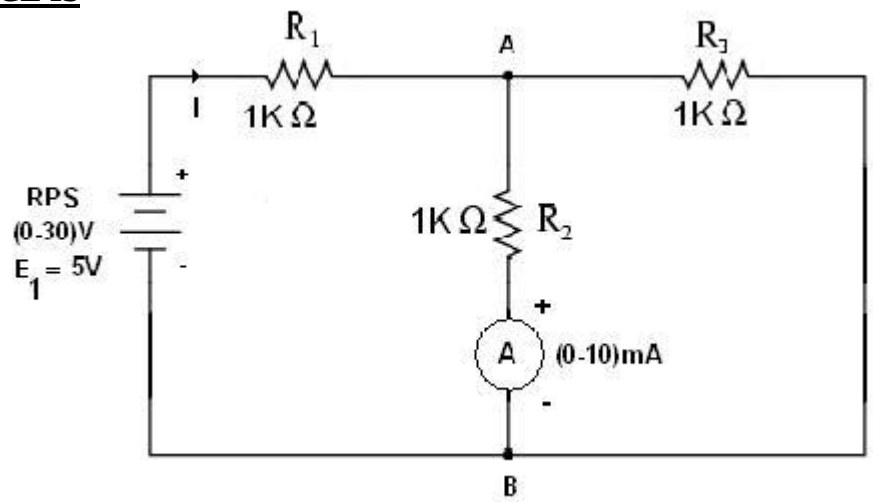


Circuit Diagram for Superposition Theorem

Table:

S.No	E**1** voltage(Volts)	E**2** voltage(Volts)	Load current across the branch AB (mA)	
			Theoritical	Practical
1				

E1 SOURCE IS



CALCULATION:

$R_1 = 1K\,\Omega$; $R_2 = 1K\,\Omega$; $R_3 = 1K\,\Omega$

$$R_T = R_1 + R_p$$

$$= R_1 + \frac{R_2 R_3}{R_2 + R_3}$$

$$I = \frac{V}{R_T}$$

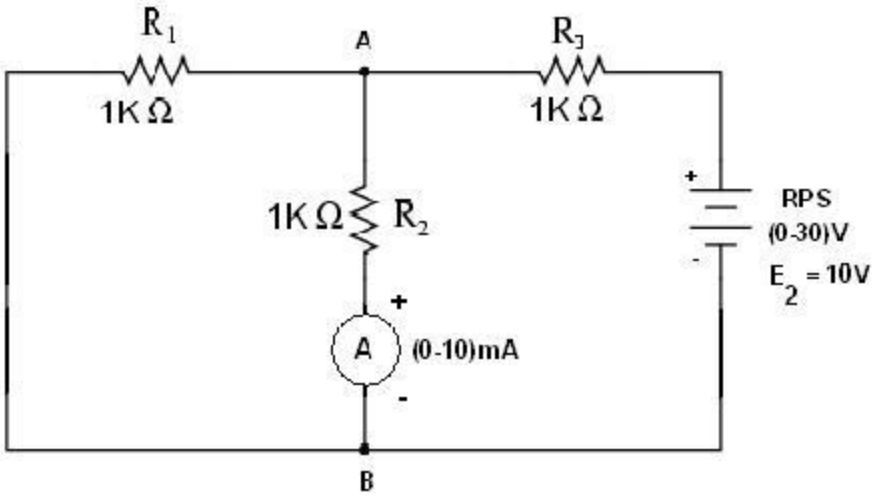
Let V = 5V,

$$I_{AB1} = I\ X\ \frac{R_3}{R_2 + R_3} = 3.3\ X\ 10^{-3}\ X\ \frac{1000}{1000+1000}$$

Table:

S.No	E**1** voltage(Volts)	Load current across the branch AB (mA)	
		Theoritical	Practical
1	5		

E2 SOURCE IS ACTING:



CALCULATION:

$R_1 = 1K\,\Omega$; $R_2 = 1K\,\Omega$; $R_3 = 1K\,\Omega$

$$R_T = R_3 + R_p$$

$$= R_3 + \frac{R_1 R_2}{R_1 + R_2}$$

$$I = \frac{V}{R_T}$$

Let V = 10V,

$$I_{AB2} = I\ X\ \frac{R_3}{R_2 + R_3} = 6.66\ X\ 10^{-3}\ X\ \frac{1000}{1000+1000}$$

Table:

S.No	E**2** voltage(Volts)	Load current across the branch AB (mA)	
		Theoritical	Practical
1	10		

E1 and E2 SOURCES ARE ACTING:

$$I_{AB} = I_{AB1} + I_{AB2}$$

RESULT:

Thus the superposition theorem for the given circuit is verified.

MAXIMUM POWER TRANSFER THEOREM

EX. NO: 11(a)

AIM:

To verify the maximum power transfer theorem for the given circuit.

APPARATUS REQUIRED:

S.NO	APPARATUS	TYPE	RANGE	QUANTITY
1	RPS	DC	(0-30)V	1
2	Resistor	-	1KΩ	2
3	Variable Resistor		1KΩ	1
4	Ammeter	DC	(0-10)mA	1
5	Bread board	-	-	1
6	Connecting wires	-	-	Few

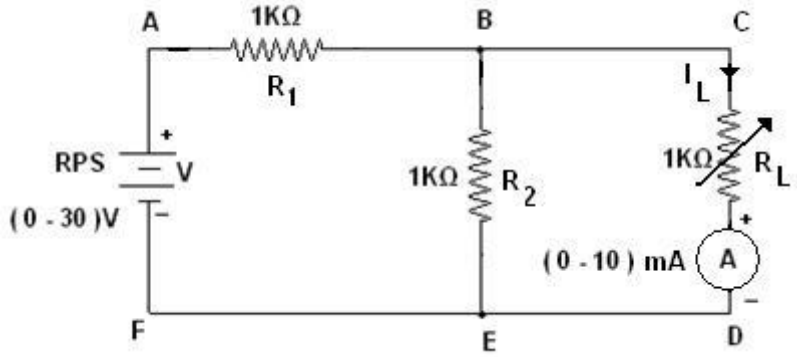
THEORY:

MAXIMUM POWER TRANSFER THEOREM:

In electrical engineering, the **maximum power (transfer) theorem** states that, to obtain maximum external power from a source to a load with a finite internal resistance, the resistance of the load must be made the same as that of the source.

The theorem applies to maximum power, and not maximum efficiency. If the resistance of the load is made larger than the resistance of the source, then efficiency is higher, since most of the power is generated in the load, but the overall power is lower since the total circuit resistance goes up.

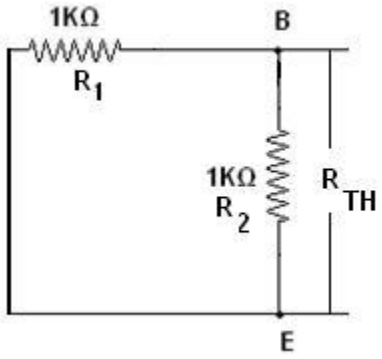
If the internal impedance is made larger than the load then most of the power ends up being dissipated in the source, and although the total power dissipated is higher, due to a lower circuit resistance, it turns out that the amount dissipated in the load is reduced.



Circuit Diagram for Maximum Power Transfer Theorem

CALCULATION:

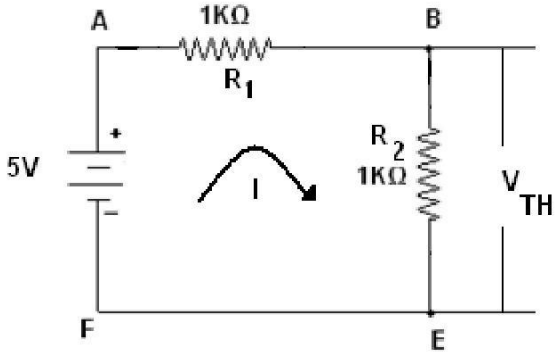
To Find RTH:



$R_1 = 1K\Omega$; $R_2 = 1K\Omega$;

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} = \frac{1000\ X\ 1000}{1000 + 1000}$$

To Find VTH:



$$I = \frac{V}{R_T}$$

Let V = 5V,

$V_{TH} = V_{BE} = 5 - 1K\ X\ I$

$\therefore I_L = \frac{V_{TH}}{2\ X\ R_{TH}} = \frac{2.5}{2\ X\ 500} = 2.5mA$

$\therefore P_{max} = {I_L}^2\ X\ R_{TH} = 2.5\ X\ 10^{-3}\ X\ 2.5\ X\ 10^{-3}\ X\ 500$

$\therefore Load\ Resistance\ R_L =$

PROCEDURE:

1. The circuit connections are given as per the circuit diagram.
2. Switch ON the power supply.
3. Initially set 5V as input voltage from RPS.
4. The ammeter reading is noted for various values of load resistance and the values are tabulated.
5. The load resistance for the maximum power is obtained from the table.

Table:

Let V = 5V

S.No	**Resistance(RL) in Ohms**	**Current(IL) in mA**	**Power (IL^2RL) in mW**
1	100		
2	200		
3	300		
4	400		
5	500		
6	700		
7	900		

RESULT:

Thus the maximum power transfer theorem for the given circuit is verified successfully.

RECIPROCITY THEOREM

EX. NO: 11(b)

AIM:

To verify the reciprocity theorem for the given circuit.

APPARATUS REQUIRED:

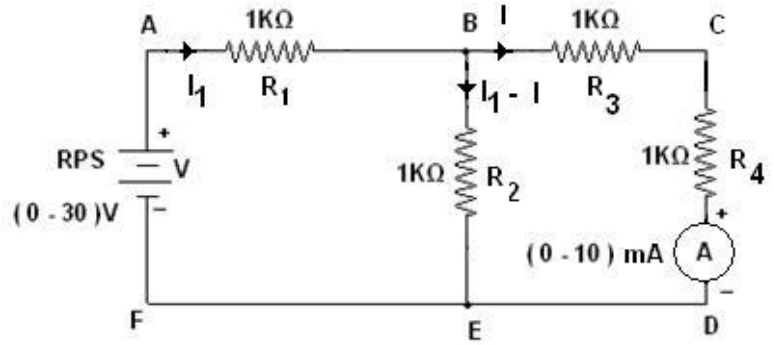
S.NO	APPARATUS	TYPE	RANGE	QUANTITY
1	RPS	DC	(0-30)V	1
2	Resistor	-	1KΩ	4
3	Ammeter	DC	(0-5)mA	1
4	Bread board	-	-	1
5	Connecting wires	-	-	Few

THEORY:

RECIPROCITY THEOREM:

The reciprocity theorem states that if an emf 'E' in one branch of a reciprocal network produces a current I in another, then if the emf 'E' is moved from the first to the second branch, it will cause the same current in the first branch, where the emf has been replaced by a short circuit. We shall see that any network composed of linear, bilateral elements (such as R, L and C) is reciprocal.

Before interchanging:



Circuit Diagram for Reciprocity TheoreM

CALCULATION:

Let V=5V

In the loop ABEF by applying KVL,

$$I_1R_1 + (I_1 - I)R_2 = V$$

$$I_1 X\ 1 + (I_1 - I)\ X\ 1 = 5$$

$$2I_1 - I = 5 - - - - - - - - - - - - - - (1)$$

In the loop BCDE by applying KVL,

$$IR_3 + IR_4 - (I_1 - I)R_2 = V$$

$$I\ X\ 1 + I\ X\ 1 - (I_1 - I)\ X\ 1 = 0$$

$$-I_1 + 3I = 0 - - - - - - - - - - - - - - (2)$$

$$D = \begin{vmatrix} 2K & -1K \\ -1K & 3K \end{vmatrix} = 6K^2 - 1K^2 = 5K^2 = 5\ X\ 10^6$$

$$D_2 = \begin{vmatrix} 2K & 5 \\ -1K & 0 \end{vmatrix} = 5K = 5\ X\ 10^3$$

$$I = \frac{D_2}{D} = \frac{5\ X\ 10^3}{5\ X\ 10^6} = 1mA$$

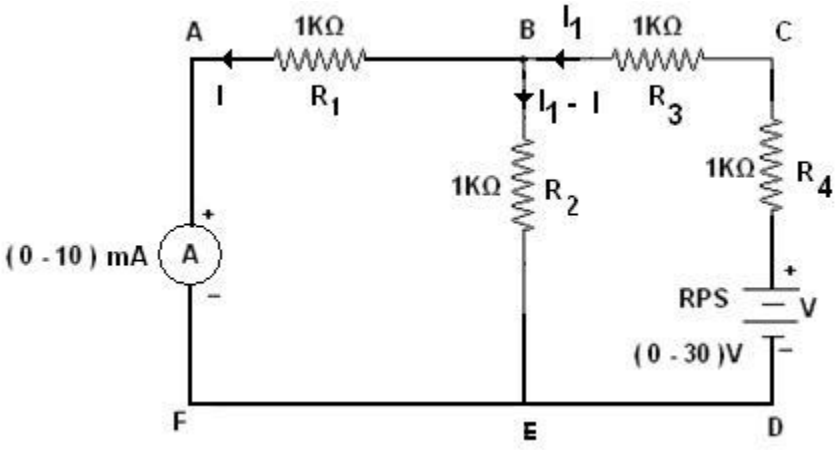
PROCEDURE:

1. The circuit connections are given as per the circuit diagram.
2. Switch ON the power supply.
3. Initially set 5V as input voltage from RPS.
4. The ammeter reading is noted and tabulated.

Table for before interchanging:

V (Volts)	Current (mA)	
	Theoritical	Practical
5		

After interchanging:



Circuit Diagram for Reciprocity Theorem

CALCULATION:

Let V=5V.

In the loop ABEFA by applying KVL,

$IR_1 - (I_1 - I)R_2 = V$

$I\ X\ 1 - (I_1 - I)\ X\ 1 = 0$

$-I_1 + 2I = 0 - - - - - - - - - - - - - - - (1)$

In the loop BCDE B by applying KVL,

$I_1R_4 + I_1R_3 + (I_1 - I)R_2 = V$

$I_1\ X\ 1 + I_1\ X\ 1 + (I_1 - I)\ X\ 1 = 5$

$3I_1 - I = 5 - - - - - - - - - - - - - - - (2)$

D = $\begin{vmatrix} -1K & 2K \\ 3K & -1K \end{vmatrix} = 1K^2 - 6K^2 = -5K^2 = -5\ X\ 10^6$

$D_2 = \begin{vmatrix} -1K & 0 \\ 3K & 5 \end{vmatrix} = -5K - 0 = -5\ X\ 10^3$

$I = \frac{D_2}{D} = \frac{-5\ X\ 10^3}{-5\ X\ 10^6} = 1mA$

PROCEDURE:

1. The circuit connections are given as per the circuit diagram.
2. Switch ON the power supply.
3. Initially set 5V as input voltage from RPS.
4. The ammeter reading is noted and tabulated.

Table for before interchanging:

V (Volts)	Current (mA)	
	Theoritical	Practical
5		

RESULT:

Thus the reciprocity theorem for the given circuit is verified successfully.

FREQUENCY RESPONSE OF RESONANCE CIRCUIT

EX. NO: 12

AIM:

To analyze the frequency response of series and parallel resonance circuits.

APPARATUS REQUIRED:

S.NO	APPARATUS	TYPE	RANGE	QUANTITY
1	Function Generator	AC	(1Hz-3MHz)	1
2	Resistor	AC	600Ω	1
3	Inductor	AC	101.4mH	1
4	Capacitor	AC	0.01mF	1
5	Ammeter	AC	(0-10)mA	1
6	Bread board	-	-	1
7	Connecting wires	-	-	Few

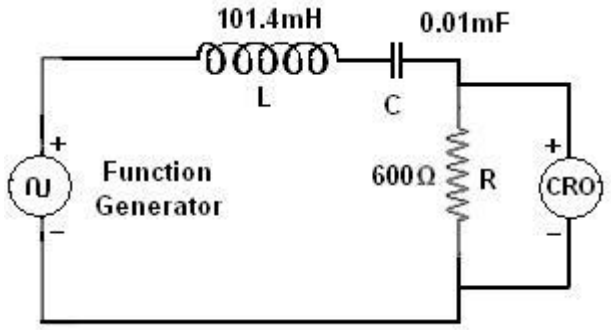
THEORY:

The resonance of a RLC circuit occurs when the inductive and capacitive reactance are equal in magnitude but cancel each other because they are 180 degrees apart in phase. The sharp minimum in impedance which occurs is useful in tuning applications. The sharpness of the minimum depends on the value of R.

The frequency at which the reactance of the inductance and the capacitance cancel each other is the resonant frequency (or the unity power factor frequency) of this circuit. This occurs at

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

SERIES RESONANCE:



Circuit Diagram for Series Resonant

CALCULATION:

R = 600Ω

L = 101.4mH

C = 0.01μF

$$\therefore The\ resonant\ frequency\ is,$$

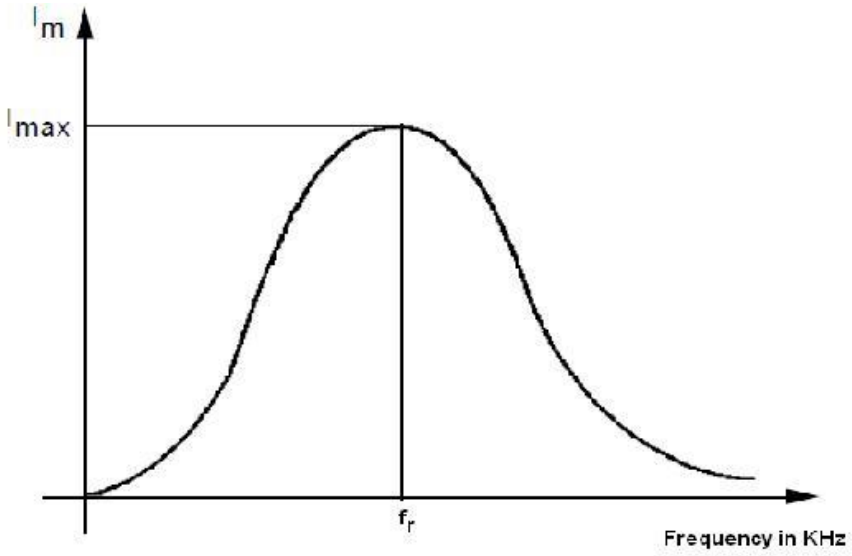
$$f_r = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{101.4\ X\ 10^{-3}\ X\ 0.01\ X\ 10^{-6}}} = 5\ KHz$$

PROCEDURE:

1. The circuit connections are given as per the circuit diagram.
2. Switch ON the power supply.
3. The input is given in the form of sin wave by function generator.
4. The amplitude of the response across the resistor is noted for various frequency ranges.
5. The current is calculated and tabulated.

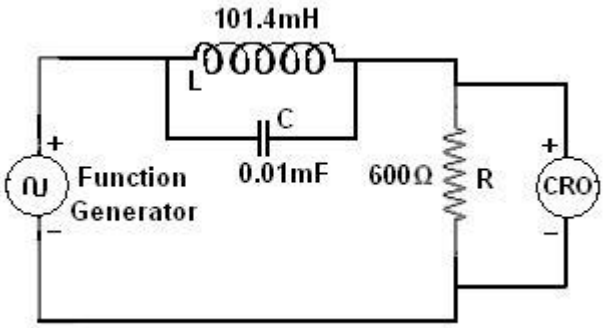
Table:

S.No	Frequncy (KHz)	Output voltage (Volts)	I = V / R (mA)
1	1		
2	2		
3	2.5		
4	3		
5	4.5		
6	6		
7	7		
8	8		



Frequency Response of Series Resonance Circuit

PARALLEL RESONANCE:



Circuit Diagram for Parallel Resonant

CALCULATION:

R = 600Ω

L = 101.4mH

C = 0.01μF

$$\therefore \textit{The resonant frequency is,}$$

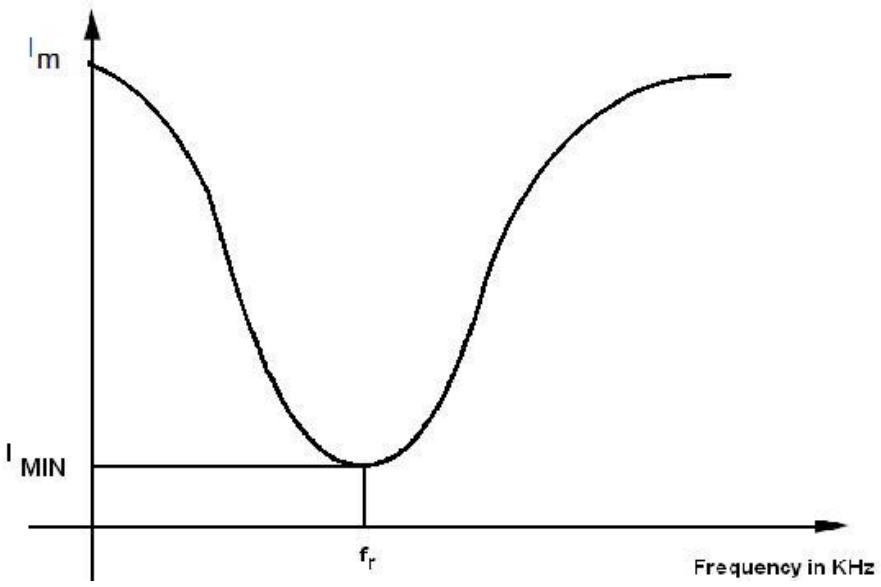
$$f_r = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{101.4\ X\ 10^{-3}\ X\ 0.01\ X\ 10^{-6}}} = 5\ KHz$$

PROCEDURE:

1. The circuit connections are given as per the circuit diagram.
2. Switch ON the power supply.
3. The input is given in the form of sin wave by function generator.
4. The amplitude of the response across the resistor is noted for various frequency ranges.
5. The current is calculated and tabulated.

Table:

S.No	Frequency (KHz)	Output voltage (Volts)	I = V / R (mA)
1	1		
2	1.8		
3	2.5		
4	3		
5	4		
6	5.2		
7	7		
8	8		



Frequency Response of Parallel Resonance Circuit

RESULT:

Thus the frequency response of series and parallel resonant circuits are analyzed